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Design and analysis of IGZO thin film transistor for AMOLED pixel circuit using double-gate tri active layer channel

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Abstract

In this research work, Amorphous Indium−Gallium−Zinc−Oxide (α-IGZO) thin-film transistor consisting of Tri-Active Layer (TAL) channel have been designed in a double-gate structure. The electrical performance of the novel device structure has been analyzed with its output and transfer characteristics, at different overlap and offset length between gate and Source-Drain (S-D) contacts. The resulted parameters have a better agreement to the device characteristics including high I_{ON}/I_{OFF} at offset of the thin-film transistor (TFT) of order 10^{11}, high channel mobility is $16.08\ cm^2/V.s$ in overlap, while it is less than $6\ cm^2/V.s$ for the offset TFTs. The superior electrical behavior of the novel double-gate TAL TFT have been incorporated. Later on, the device application in a new Active Matrix −Organic Light Emitting Diode (AMOLED) pixel circuit has been proposed.

Keyword: Electrical engineering

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1. Introduction

Transparent amorphous conducting oxide thin films have been considered for various application areas such as switching element in backplane of flat panel displays. Among the Transparent Conducting Oxides (TCOs) Amorphous-Indium Gallium Zinc Oxides (α-IGZO), as active channel layer of TFT, have become more popular in comparison to the conventional amorphous oxide materials. The TFT device behavior mainly depends on channel layer particularly within *1 nm−2 nm* of the interface layer irrespective of the substrate used [1, 2] and the electron mobility, electron concentration, density of state, and interfacial charge directly influence the field-effect mobility, I_{ON}/I_{OFF} ratio, sub-threshold swing, and turn-ON voltage of the device. The α-IGZO has wider energy band-gap which offers good transparency in the visible spectrum, peculiar chemical bonding instigates high field mobility, and display improved electrical characteristics such as high I_{ON}/I_{OFF} ratio, enhanced lifetime, better transmittance, and optimum large-area uniform integration [3, 4]. However, Indium (*In*) and Gallium (*Ga*) contents in the active layer decide the electrical properties in the α-IGZO based TFTs. The increase of *In* contents enhances the mobility but result in increased OFF-current undesirably, which deteriorates the sub-threshold swing. In contrary, the increase of *Ga* content decreases OFF-current, provides improved sub-threshold swing, but diminishes the mobility parameters [5]. The single-active layer has inherent limitations, therefore, it possesses low film density and hence multi-stack layer channel structure of TFTs have been proposed to overcome the limitations. The first bilayer/double-active layer structure introduced by Kim et al. [6] was intended to resolve all those issues. Fundamentally, in bilayer/double-active layer TFTs, high-mobility semiconductor is complemented with low carrier concentration of Amorphous Oxide Semiconductors (AOS). It is useful for achieving higher mobility and stability as compared to the single-active layer channel structure, because both the front and back-channels inhabits high charge trap density and carrier concentrations [7, 8]. Subsequently, several other double-active layer combinations e.g. ITO−IGZO, IZO−IGZO, IZO−ZTO, and IZO−AIZTO etc. exists. However, ITO−IGZO combination attained more focus due to very small interface trap density (d_{it}), existence of smoother surface in both layers, and the homo-junction formation by ITO and α-IGZO [9]. Moreover, based on the solid-state energy scale oxygen anion-derived valence band makes almost equal ionization potential and same band-gap for both the ITO and α-IGZO thin films [10]. The typical thickness for high mobility layer ranging between *3 nm* and *6 nm* have been researched for a *30 nm* thick low carrier concentration layer for the optimum results [7, 11, 12]. In previous researches, single gate α-IGZO based TFTs with double layer active channel have reported for improved electrical characteristics [8, 9, 13]. But α-IGZO TFT in Double-Gate (DG) structure has more prospects in circuit design due to the control of threshold voltage using bias at Top Gate (TG). In DG TFTs, the primary and secondary gate are Bottom Gate (BG) and Top Gate (TG), respectively that are

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biased individually at increasing BG terminal from negative to positive voltage. It has been reported in the past that utilizing two gates in device makes stronger electrostatic control over the channel and drain field do not affect or disrupt the channel. In addition, double-gate structure reduces OFF-state current due to the second gate, and hence increases the overall current ratio I_{ON}/I_{OFF} with enhanced electrical characteristics [14]. The top contact bottom gate structures are usually designed with an overlap between gate and S-D conductors [15], which originates kick-back potential, high noise, and delayed response of TFT display array [16, 17, 18] due to existence of overlap capacitance in the device. However, overlap capacitance can be eliminated by creating offset in active matrix displays with trivial kickback voltage [19, 20, 21], but at the cost of dropping down of drain current.

In this present work, authors have proposed a novel Double-Gate Tri Active Layer channel (DG-TAL) Thin Film Transistor and analyzed its output and transfer characteristics at different overlap and offset length between gate and S-D contacts. The electrical parameters of the device have been reported and its application in AMOLED pixel circuit are realized. This work has been organized as follows: Section 2 describes the device design specification and simulation parameters. Section 3 discusses the results of the designed device and present the circuit application. Finally, Section 4 concludes the work and recommends the future aspects.

2. Design

The schematic of the proposed top contact, bottom-gate thin film transistor structure is shown in Fig. 1. The bottom gate insulator SiO_2 of thickness *130 nm* is deposited

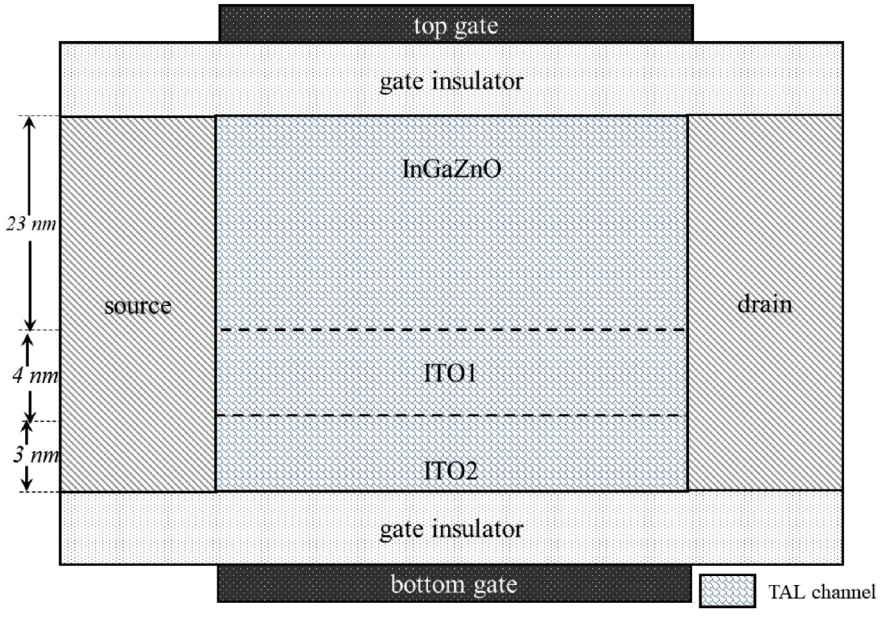

Fig. 1. Schematic of the proposed device structure.

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above a heavily doped p-type Silicon substrate. A *30 nm* thick active layer consisting of α-IGZO and Tin doped Indium Oxide (ITO) has been deposited as the channel of TFT, keeping *25 μm* of channel length. The *30 nm* thick active channel layer is formed of sublayer of *23 nm* α-IGZO, *4 nm* by an ITO layer-1 (ITO1), and *3 nm* of ITO layer-2 (ITO2). Predominantly, the sublayer ITO2 differ from ITO1 by means of lower carrier concentration of $3.63 \times 10^{14}\ cm^{-3}$. The layer thickness and doping concentration provide greater control on the device characteristics. The third sublayer of the active channel with lower concentration provide higher charge trap density, and increases the mobility of channel structure. For creating double-gate structure another layer of *130 nm* thick SiO_2 has been deposited for top gate insulator. At the same time, Molybdenum (*Mo*) metallic contacts are selected for top and bottom gate biasing.

The material physical parameters used in this simulation model are given in Table 1. The Density of States (DOS) profile is then outlined and adjusted till the simulation convergence. The probe is positioned near the dielectric-channel interface aligned to the width. Fig. 2 depicts the DOS model and simulation parameters for IGZO and ITO used in this work adapted from [24, 25, 26] are shown in Table 2.

3. Results & discussion

Double-Gate Tri-Active Layer (DG TAL) channel TFT have been simulated to analyze the overlap and offset length effect on drain current of the device. As the result of simulation contour plot of field distribution in channel region has been obtained. Fig. 3 shows field distribution at $V_{G(top\ gate)} = 0\ V$ and $V_{G(bottom\ gate)} = 20\ V$ with overlap length of *2 μm* and offset of *1.5 μm* and *2.5 μm*, respectively. It is apparent from Fig. 3 that at overlap of gate and Source/Drain (S/D) electrodes, the entire TAL channel is accumulated, whereas the accumulation diminishes near S/D electrodes at increasing offset lengths of *1.5 μm*, and 2.5 μm. The substantial variation in the conduction length along the length of the channel has been clearly

Table 1. Key physical parameters.

Parameters	IGZO	ITO
Bandgap (E_g)	3.2 *eV*	_
Density of state electron effective mass (m_e) [22, 23]	0.34	0.30
Electron band mobility (μ_p)	15 $cm^2/V.s$	35 $cm^2/V.s$
Hole band mobility (μ_p)	0.1 $cm^2/V.s$	_
Electron affinity (χ)	4.16 *eV*	4.16 *eV*
Carrier concentration (N)	_	$3.63 \times 10^{14}\ cm^{-3}$ $3.63 \times 10^{18}\ cm^{-3}$

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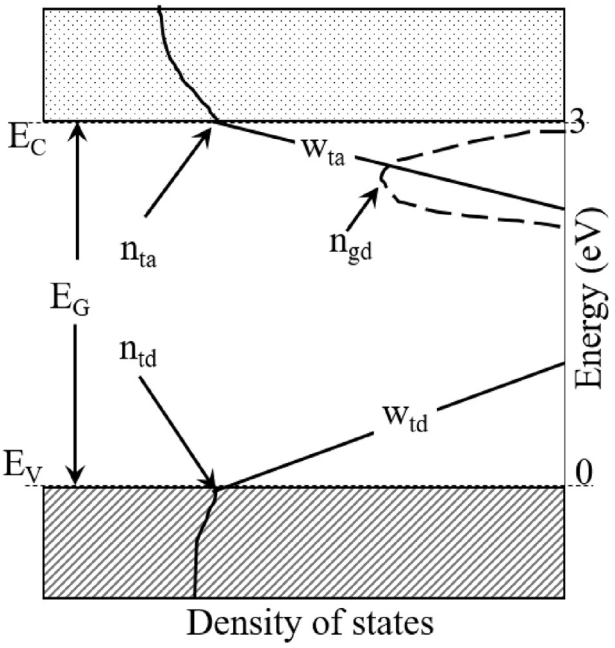

Fig. 2. Density of state (DOS) model for α-IGZO.

Table 2. DOS simulation parameters.

Parameters	IGZO	ITO
Peak density, donor band-tail states (n_{td}, cm^{-3}/eV)	1.55×10^{20}	1.55×10^{20}
Peak density, acceptor band-tail states (n_{ta}, cm^{-3}/eV)	1.21×10^{20}	2.20×10^{20}
Urbach energy (donor band-tail) (w_{td}, meV)	110	110
Urbach energy (acceptor band-tail) (w_{ta}, meV)	30	18
Peak energy (Gaussian donor) (E_{gd}, eV)	2.95	_
Peak energy (Gaussian acceptor) (E_{ga}, eV)	1.2	_
Peak density (Gaussian donor) (n_{gd}, cm^{-3}/eV)	1.6×10^{16}	_
Peak density (Gaussian acceptor) (n_{ga}, cm^{-3}/eV)	3.2×10^{17}	_
Decay energy (Gaussian donor) (w_{gd}, eV)	0.1	_
Decay energy (Gaussian acceptor) (w_{ga}, eV)	0.1	_
Interface-trap density (d_{it}, cm^{-3}/eV)	6.0×10^{11}	6.0×10^{10}

observed at constant bottom gate voltage. Consequently, the drain current reduces due to decrease in carrier accumulation in the channel region at offset and the trend increases with increasing offset length.

As the performance of TFTs are characterized by I-V characteristics, the electrical parameters have been further extracted from the output and transfer characteristics curve as follows:

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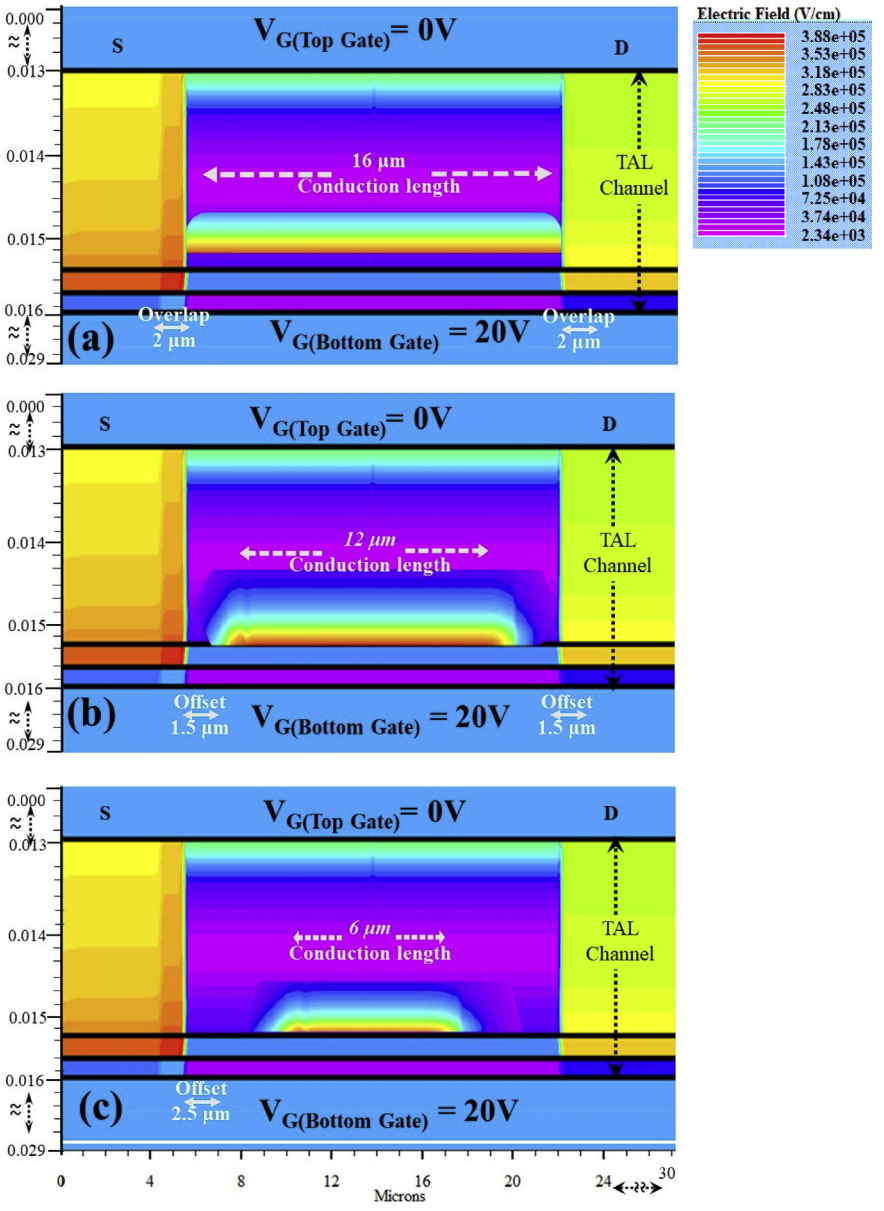

Fig. 3. Electric field in (DG) TAL-TFTs (a) overlap *2 µm* (b) offset *1.5 µm* (c) offset *2.5 µm*.

3.1. Output characteristics

The applied gate voltage (V_G) changes the drain current (I_D) at increasing values of drain voltage (V_D). Therefore, series of curves for the discrete values of V_G can be obtained. Fig. 4 (a) shows the output characteristic of DG-TAL channel TFT at the overlap length of *2 µm* with bottom gate bias (V_{BG}) of *10 V at* top gate bias (V_{TG}) increments of *10 V* ranging from -20 *V* to $+20$ *V*.

The graph shows active, pinch-off and saturation region and promising results with typical transistor theory. The operation revealed the fact that only a small drain current

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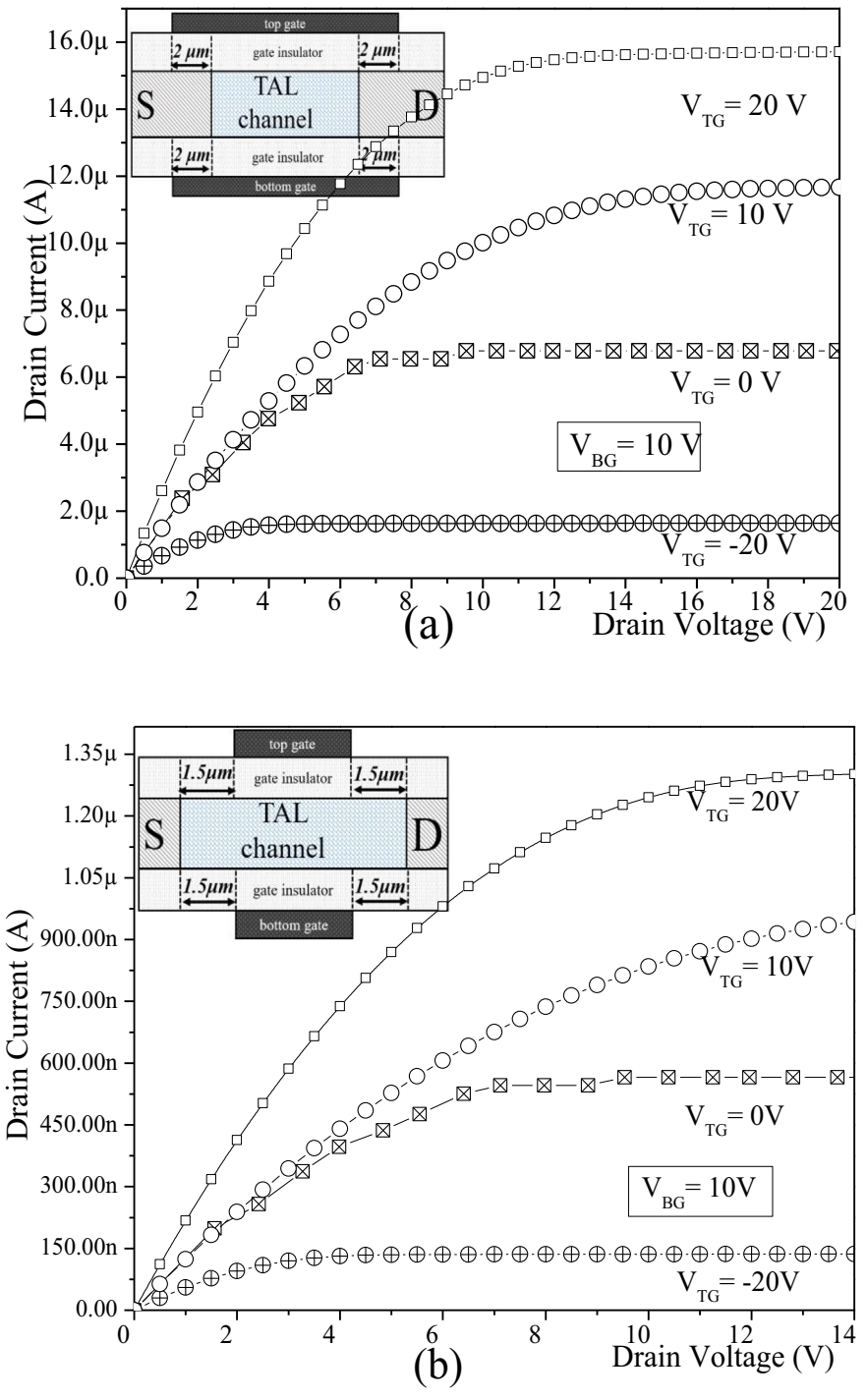

Fig. 4. Output characteristics of DG TAL-TFTs (a) overlap *2 μm* (b) offset *1.5 μm*.

exists at $V_{TG} = 0\ V$ in the overlap case with positive V_{BG} generate carriers and tempted conducting channel with channel conductivity increased by positive V_{TG}. However, in another case with offset structure produce even lower OFF current in linear region yet slight decrease in saturation current at higher V_{TG} and V_D as shown in Fig. 4 (b).

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3.2. Transfer characteristics

The parameters used for describing the performance of TFTs are extracted from the transfer characteristic. The transfer characteristic is obtained when the gate bias is swept at fixed drain voltage, selected to ensure that the device working in saturation region ($V_D \geq V_G$ - V_{TH}). Fig. 5 shows the transfer characteristics of the device with DG bias at overlap (*2 μm*) and offset (*1.5 μm*). It has been observed in Fig. 5(a) that the drain current rises exponentially after the certain threshold voltage. The current increases as the channel at increasing threshold value becomes wider, and allow more charges to pass through between source and drain of the TFT. In case of the offset between the electrodes, lower OFF current has been achieved as shown in Fig. 5(b), while the overlap displays the higher drain current due to the larger conduction length.

3.3. Extraction of electrical parameters

The distinct parameters describe the performance of TFTs, which include field-effect mobility (μ_{FE}), current-ratio (I_{ON}/I_{OFF}), threshold voltage (V_{TH}), and sub threshold voltage swing, which are derived from the I-V characteristics curves. The μ_{FE} is accountable as the channel mobility of thin film transistor determined from the drain current in the linear region of the device operation [26], as given in Eq. (1).

$$I_D = \mu_{FE} C_{DG} \frac{W_{ch}}{L_{ch}} (V_G - V_{TH}) V_{DS} \tag{1}$$

where W_{ch} and L_{ch} are the width and length of TFT channel, and C_{DG} is the gate capacitance per unit area.

In the DG structure, two capacitance regions are formed, one between channel and top gate and the other is channel and bottom gate as C_{TG} and C_{BG}, whose values are depending upon thickness. If the top and bottom gate dielectric thicknesses are d_{TG} and d_{BG} with dielectric constants ε_{BG} and ε_{BG}, respectively, then $C_{TG} = \varepsilon_{TG}/d_{TG}$, and $C_{BG} = \varepsilon_{BG}/d_{BG}$. The capacitance in DG-structure (C_{DG}) cannot be directly determined but can approximated as the sum of C_{TG} and C_{BG} as the two capacitances are formed in parallel overall [27]. Therefore, $C_{DG} = C_{TG} + C_{BG}$.

The Subthreshold Slope (SS) as given in Eq. (2), is the slope in transfer characteristics in the linear portion of a MOS device characteristics [26].

$$SS = \left(\frac{\partial \log I_D}{\partial V_G} \right)^{-1} \tag{2}$$

The SS parameter of the double-gate TAL TFT structure, derived from capacitive model [28] is calculated using Eq. (3).

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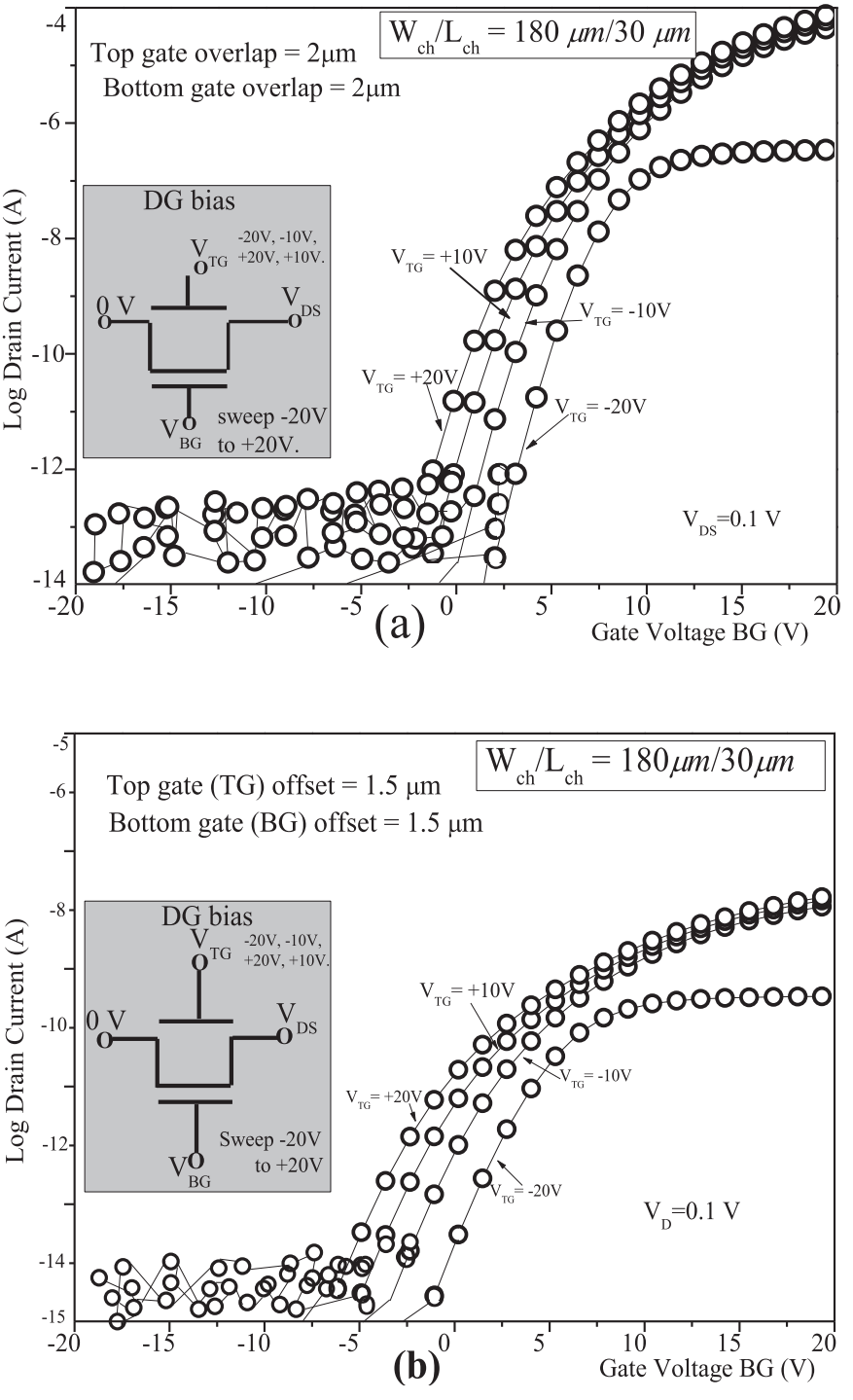

Fig. 5. Transfer characteristics of DG TAL-TFTs (a) overlap *2 μm* (b) offset *1.5 μm*.

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$$SS \cong \left(\frac{kT}{q}\right)\ln_{10}\left(1+\frac{C_{BI}+C_{TI}}{C_{BG}+C_{TG}}\right) \quad (3)$$

where k, T, and q are the Boltzmann constant, temperature, and charge of electron, respectively and C_{BI} and C_{TI} are the capacitance of the bottom and top channel interface states. C_{BI} and C_{TI} is defined by $C_{BI} = q.N_{BIT}$ and $C_{TI} = q.N_{TIT}$, where N_{BIT} and N_{TIT} denotes density of bottom and top interface trap states. The average interface trap density (N_{IT}) can be assumed equal to N_{BIT} and N_{TIT}.

The I_{ON}/I_{OFF} is the quantitative amount which describes switching efficiency of TFT signifies the ratio of largest current to lowest current of its operation at different gate voltages can be determined by assessing the drain currents in the transfer-characteristics. The extracted parameters of DG TAL TFT for the overlap and offset structures and comparison with the coplanar DG TFT [28] are listed in Table 3. Comparably, the obtained results of DG TAL TFT shows that at double-gate bias V_{TH} is (*0.28 V* in overlap and *0.06 V* in offset) significantly lower, μ_{FE} is *3 cm^2/Vs* higher in overlap, equivalent $I_{ON}/I_{OFF,}$ and SS are obtained in comparison to the DG Coplanar TFT.

3.4. Application of DG-TAL TFT in AMOLED pixel circuit

In the AMOLEDs Pixel circuit, α-IGZO TFTs have been prominent due to its notable advantages i.e. high mobility, stability and low temperature processing. AMOLED pixel driver circuit using double-gate TFTs have been proposed to overcome electrical instability issues of Single Gate TFTs which in turn causes threshold voltage shift when subjected to continuous gate bias-stress. V_{TH} shift results in substantial OLED current degradation and brightness deterioration. Hence the circuit using double-gate TFTs have been introduced in past for threshold shift compensation [29, 30, 31, 32]. The double-gate structure in α-IGZO TFTs displays even much improved characteristics including a high I_{ON} current, significant subthreshold swing, and good control of the threshold voltage. A conventional pixel circuit using

Table 3. Extracted electrical parameters of DG-TAL TFT at S/D overlap and Offset and comparison with coplanar DG-TFT.

Parameter (*Unit*)	Gate and S/D Overlap length 2 μm			Gate and S/D Offset length 1.5 μm			Gate and S/D in Coplanar Structure		
	Top gate bias	Bottom gate bias	Double-gate bias	Top gate bias	Bottom gate Bias	Double-gate Bias	Top gate bias	Bottom gate Bias	Double-gate Bias
V_{TH} (*V*)	0.80	0.55	0.27	−0.64	0.79	0.49	0.42	0.54	0.55
I_{ON} (*μA/μm*)	9.2	6.13	2.9	9.23	0.45	3.1	0.63	1.3	2.0
I_{OFF} (*nA/μm*)	3.2×10^{-6}	1.7×10^{-6}	3×10^{-4}	4.9×10^{-5}	1.3×10^{-5}	2.2×10^{-8}	$<1.0 \times 10^{-4}$	$<1.0 \times 10^{-4}$	$<1.0 \times 10^{-4}$
SS (*V/decade*)	0.297	0.162	0.107	0.283	0.171	0.199	0.286	0.153	0.100
μ_{FE} ($cm^2/V.s$)	12.79	13.82	16.08	4.21	9.11	6.07	11.52	12.8	13.08

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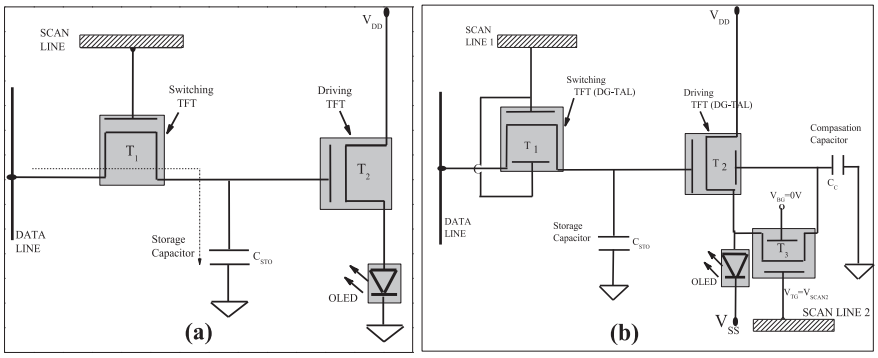

Fig. 6. AMOLED pixel circuit (a) conventional TFT (b) Proposed (DG)TAL α-IGZO based TFT.

double-gate is comprised of two TFTs and a capacitor as shown in Fig. 6 (a) [33], which has one T_1 (Switch-TFT) and the other is T_2 (Drive-TFT). The T_1 switches ON and OFF in program interval and capacitor gets charged up to data voltage level. In its ON state, T_2 supplies constant current for driving OLED from the capacitor (C_{STO}) voltage. If the capacitor is not fully charged with in the program interval, it leads to display error. Hence the switching TFT must have higher I_{ON}/I_{OFF} ratio for faster switching. As the designed DG-TAL TFT in offset structure has shown low OFF current along with superior electrical parameters, it will certainly be improving the charging performance of capacitor in the pixel circuit. Fig. 6(b) shows the AMOLED pixel circuit utilizing DG-TAL TFT has been proposed as shown in with two DG-TAL TFTs and one capacitor as switching, driving, and, storage element, respectively. An additional control line is needed to independently bias the top gate for achieving better controllability of the V_{TH}. Hence, a sub-circuit with one capacitor (C_C), a top gate TAL TFT and two control line are added for attaining good control of threshold voltage and compensation in the proposed AMOLED pixel circuit.

4. Conclusions

The Tri-Active layer channel in α-IGZO thin film transistor with double-gate have been designed and simulated to inspect the offset length impact on the drain current. The proposed DG-TAL TFT have displayed large field effect mobility (μ_{FE}) *12.79*, *13.82* and *16.08 cm*^{2}*s/Vs* in TG, BG and DG biasing when the gate and source-drain (S/D) electrodes overlapped with *2 μm* length. At the same time offset of *1.5 μm* length have resulted in the reduced μ_{FE} *of 4.2, 9.11, and 6.07 cm*^{2} s/*V- s.* The performance analysis of the proposed DG structure gives insight to the effects of electrode overlap and offset on the electrical parameters. The DG-TAL TFT shows superior characteristics though poor subthreshold probably due to the device channel design, yet comparable to the previous reported device structure in double-gate bias condition, hence suitable and proposed as the switching transistor. Finally, a novel

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AMOLED pixel circuit have been proposed with Double-Gate Tri-Active Layer (DG TAL) channel IGZO TFTs. The other electrical parameters were obtained much better for overcoming brightness decay and V_{TH} shift compensation. In future improvement in the SS for this device structure can be worked upon. Also the performance analysis of the circuit using DG-TAL TFT can be explored for RF circuits and thin film antenna circuit design [34, 35].

Declarations

Author contribution statement

Shashi K. Dargar: Conceived and designed the experiments; Performed the experiments; Analyzed and interpreted the data; Contributed reagents, materials, analysis tools or data; Wrote the paper.

Viranjay M. Srivastava: Analyzed and interpreted the data; Contributed reagents, materials, analysis tools or data.

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Competing interest statement

The authors declare no conflict of interest.

Additional information

No additional information is available for this paper.

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