Journal of Medical Systems (2019) 43: 78
https://doi.org/10.1007/s10916-019-1186-8

IMAGE & SIGNAL PROCESSING

Asynchronous Adaptive Threshold Level Crossing ADC for Wearable ECG Sensors

Anita Antony[1] · Shobha Rekh Paulson[1] · D. Jackuline Moni[1]

Received: 22 November 2018 / Accepted: 30 January 2019 / Published online: 13 February 2019

Abstract

The level crossing ADC generates digitized samples consisting of the magnitude of input signal and time interval between two consecutive level crossings when the input signal crosses the threshold level. This paper presents a new architecture of low power asynchronous adaptive threshold level crossing (LC) ADC suitable for wearable ECG sensors based on a novel algorithm for determining adaptive threshold. The adaptive threshold was determined by calculating the mean of maximum and minimum values of signal in a predetermined window. Polynomial interpolation was used to reconstruct the signal. A signal to noise distortion ratio of 57.50 dB and a mean square error (MSE) measure of $1.368*10^{-8}$ V^2 was achieved by the proposed algorithm for a 1 mV, 10 Hz input sinusoidal signal in MATLAB. The asynchronous adaptive threshold LC ADC operating from a supply voltage of 0.8 V occupied a layout area of 266.33*331.385 μm^2 when implemented in CADENCE virtuoso using 180 nm technology. The designed circuit consumes an average power of 367.6 nW for a 1mVpp, 10 Hz input sinusoidal signal when simulated in Virtuoso.

Keywords Asynchronous · Adaptive · LC · Level crossing · ADC · Analog to digital converter · ECG · Electrocardiogram · Wearable · Sensors · Low power

Introduction

The advent of personalization of medical treatment has brought wearable technology to forefront. Personalized and customized forms of medicine administration will become more effective with the help of wearable sensors. This will reduce the risk and also reduce the treatment cost for individual patients. Wearable sensors require their batteries to have a longer battery life and smaller area for the convenience of the customer.

This article is part of the Topical Collection on *Image & Signal Processing*

✉ Anita Antony
anitaantonywork@gmail.com

Shobha Rekh Paulson
shobhapaulson@karunya.edu

D. Jackuline Moni
moni@karunya.edu

[1] Department of Electronics and Communication Engineering, Karunya Institute of Technology & Sciences, Coimbatore, India

The ECG acquisition module in the wearable ECG sensor acquires the signal and passes it to the proposed LC ADC after amplification and filtering. The block diagram of the wearable ECG sensor is shown in Fig. 1. Lower power consumption, lower supply voltage and smaller size are the desirable qualities in ADCs to be used in wearable ECG sensors. The conventional wearable ECG sensors use power hungry synchronous uniform sampling ADCs. These ADCs transmit more samples which burden the transmission system. Signal compression stages can be added to the sensor to reduce the number of samples. But this results in increased power consumption and area. LC ADC described in this paper is a promising alternative to the synchronous ADC for a sparse signal in time domain like ECG in terms of power, samples and area [1]. In level crossing sampling shown in Fig. 2, samples are generated only when the input signal crosses the threshold level. The threshold level can be a fixed threshold [2–5] or adaptive threshold level [6–8]. The magnitude of the input signal and the time between the consecutive level crossings are quantized and encoded in uniform steps using the up or down counter [9] and time to digital converter. Digitized codes from the up/down counter give the direction of level crossing and amplitude information. Timer gives the time elapsed since the

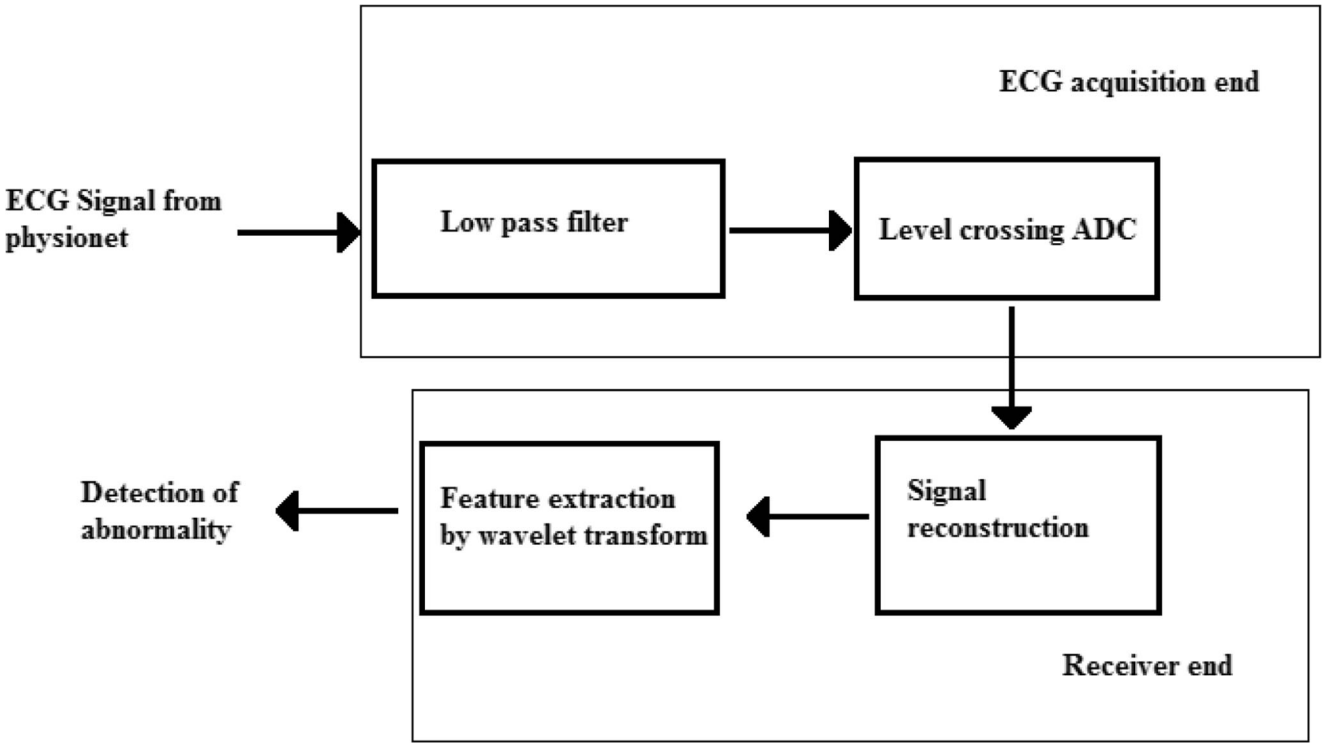


Fig. 1 Block diagram of the wearable ECG sensor

previous sample. This information can be synchronized to reconstruct the sample [4, 9, 10]. For a LC ADC, the threshold levels need to be optimally placed in the dynamic range of the input signal to prevent information loss. If more threshold levels are used, more samples than necessary will be generated [11]. So the optimal placement of threshold levels is of major concern in the design of LC ADCs. This explains the relevance of adaptive determining of the thresholds in LC ADCs.

The digitized codes can be transmitted to the external hardware wirelessly where the ECG signal is reconstructed. Heart rate and heart rhythm abnormalities (arrhythmia's) can be obtained from the reconstructed ECG signal using different classification methods, cited in previous literature, such as wavelet transform [12], autoregressive modelling [13], radial basis function (RBF) neural networks [14] and nonlinear principal component analysis neural networks [15].

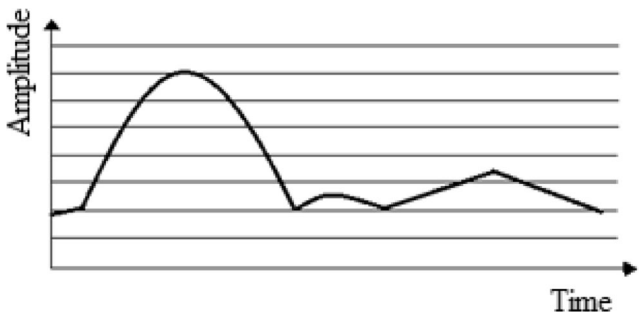


Fig. 2 Level crossing sampling

This paper implements a low power asynchronous adaptive threshold level crossing ADC based on a novel threshold determining algorithm suitable for a wearable ECG sensor. Adaptive threshold of the LC ADC is obtained by calculating mean of the maximum and minimum of the input signal in a predetermined window. The proposed algorithm is implemented using a main comparator operating at an average sampling rate of Fs Hz and a threshold determining circuitry using 180 nm technology in CADENCE virtuoso. The designed LC ADC is termed asynchronous because it employs irregular sampling and do not use a global clock. Since the sampling is nonuniform, the sampling frequency is variable and dependent on number of quantization levels and input signal amplitude variations. The LC ADC generates samples whenever the input signal crosses the adaptively determined threshold from the input signal and these time instants must be recorded. If implemented in a clock less fashion, EMI can be further reduced. The digitised code from the ADC can be transmitted to an external module which is not analysed in this paper. Assuming an error free transmission, the nonuniform sample sequence is transformed to uniform sample sequence by estimating the values between data points using polynomial interpolation for signal reconstruction and interpolation in MATLAB. The case studies of heart rate and heart rhythm abnormality detection was performed using the proposed asynchronous adaptive threshold LC ADC to prove the functionality of the design.

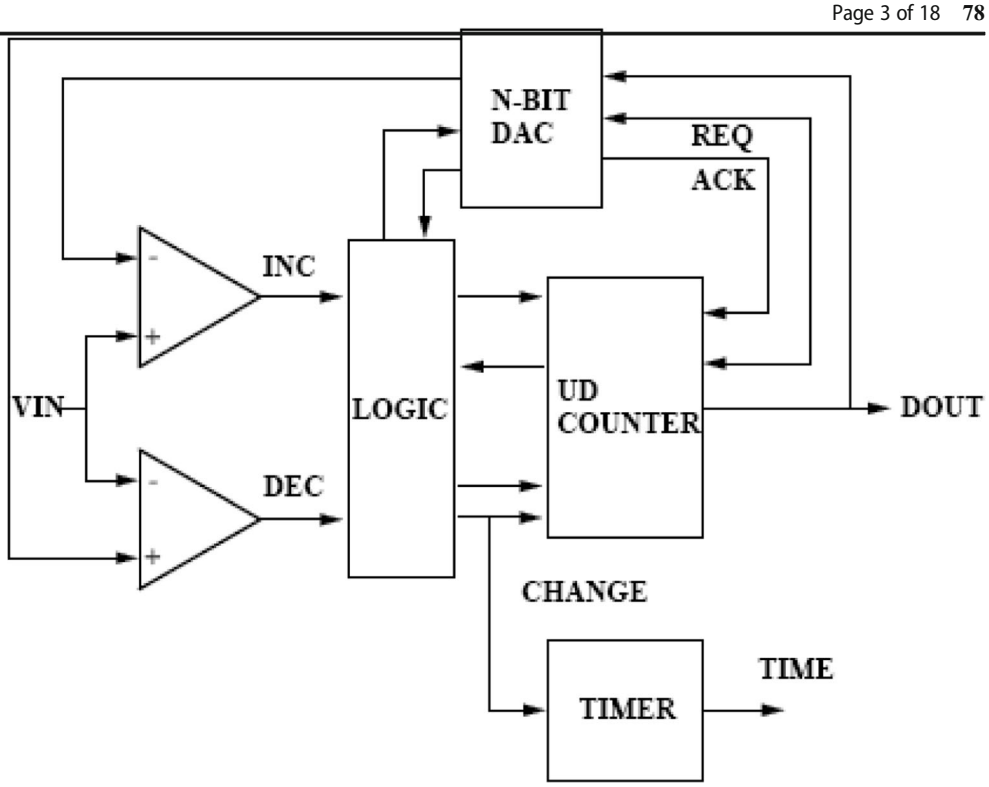


Fig. 3 General LC ADC architecture using feedback DAC

This paper is organized as follows. Section 2 surveys the previous literature on asynchronous LC ADCs. Section 3 contains the algorithm for asynchronous adaptive threshold LC ADC. Section 4 gives circuit implementation. Section 5 explains feature extraction and diagnosis of abnormality from ECG. Section 6 gives the results and discussion. Finally, conclusion and future work is given in Section 7.

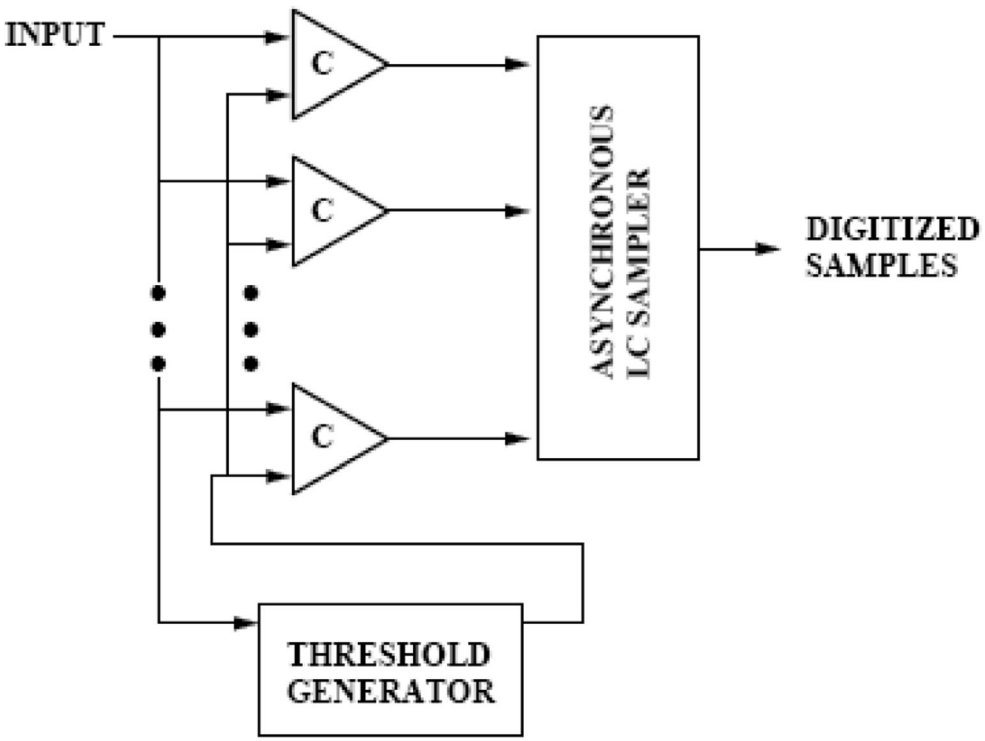


Fig. 4 General architecture of a LC ADC with FLASH ADC like architecture

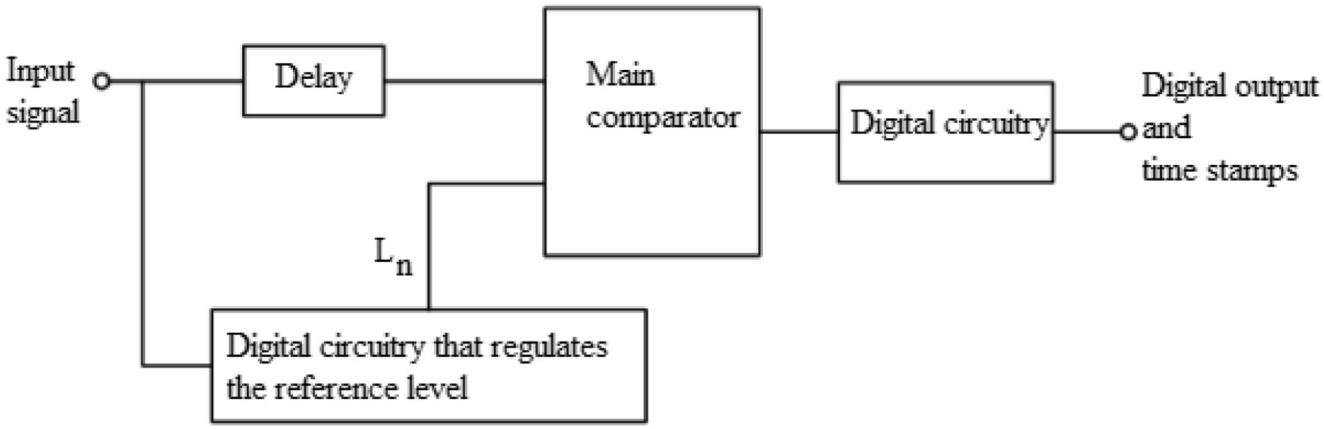


Fig. 5 Conceptual design diagram of the proposed asynchronous adaptive threshold LC ADC

Previous literature

LC ADC architectures in previous literature can be generally classified into two types: LC ADC using feedback DAC [1, 8, 9, 16, 17] and LC ADC with FLASH ADC like architecture [2, 5, 7, 11]. A general architecture of LC ADC using feedback DAC is shown in Fig. 3. They usually consist of feedback DAC, comparators, counter and timer as shown in the Fig. 3. The feedback loop with the DAC keeps the comparison window of the comparators around the input signal. The power consumption of DAC and comparator dominates the overall power consumption. The benefits of the DAC are rail to rail input swing, decreased settling time, decreased leakage and decreased output drift. The general architecture of a LC ADC with FLASH ADC like architecture is shown in Fig. 4. The comparators shown in the circuit compares the input signal with the corresponding threshold levels generated by resistive or capacitive circuit [2, 5] or by sequential algorithmic circuitry [7, 11]. The power consumption of such an analog circuitry is dominated by the number of comparators and the resistor strings or capacitor arrays. The number of the comparators used is determined by the number of threshold levels used. This directly determines the minimum voltage difference the ADC can detect. The absence of the feedback loop gives more stability to the FLASH type LC ADC.

Table 1 Algorithm

Algorithm 1: Threshold determining algorithm for level crossing ADC

Step 1.1:Initialize the update interval for determining the threshold of LC ADC, v; initialize N = T/v for an input signal of length T seconds;
Step 1.2:Resample the input signal x_t to $\tilde{x}_t$ at F_s Hz, $t_s = 1/F_s$ seconds; initialize $m = v/t_s$;
Step 1.3:For *n* = 1:N do
For i = (n-1)m + 1:nm do
select the threshold L_n such that

$$L_n = (\text{maximum}(\tilde{x}_t(i)) + \text{minimum}(\tilde{x}_t(i)))/2; \quad (4)$$

End for;
Step 1.4:Use the selected threshold to sample $\tilde{x}_t$ in the interval [(n-1)m + 1,nm] and obtain the sample set $\{Q(s_i),\lambda_i\}$;
Step 1.5:Use the sample set $\{Q(s_i), \lambda_i\}$ to obtain the reconstructed signal using polynomial interpolation;

Algorithm for asynchronous adaptive threshold LC ADC

This paper presents the algorithmic implementation of a LC ADC which can be implemented with a main comparator of average sampling frequency F_s. The main comparator compares the input with threshold levels updated every v seconds. When the input signal crosses the threshold level, digital codes and times tamps are respectively generated by the up/down counter and timer in the digital circuitry. The conceptual design diagram of the proposed asynchronous adaptive threshold LC ADC is illustrated in Fig. 5.

For an initially assumed update interval of v seconds, the input signal x_t of length T seconds is resampled to $\tilde{x}_t$ at a sampling frequency of F_s Hz, where $t_s = 1/F_s$ seconds and $t_s << v$. The design requires the input signal to be seen by the threshold determining circuitry beforehand. This is achieved by introducing a delay of v seconds before the input signal is given to the main comparator. The threshold is determined by calculating mean of the maximum and minimum of the input signal in an interval of v seconds between every threshold updates. The ADC compares the input signal with the threshold L_n every t_s seconds where L_n belongs to the set $\{L_1, L_2, \ldots L_{T/v}\}$. A level crossing is detected by the circuitry if the following

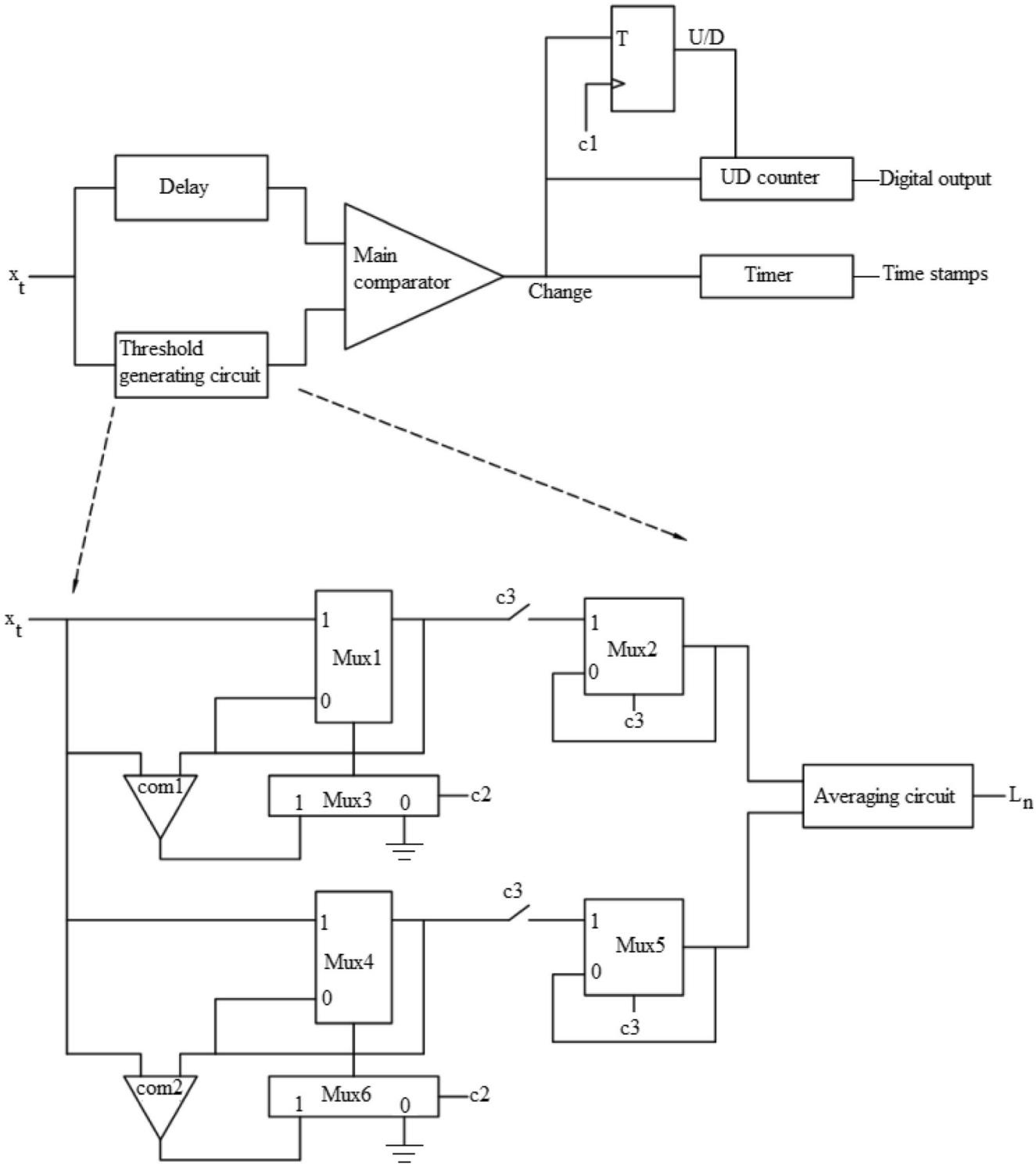


Fig. 6 Proposed LC ADC

comparison holds true.

$$\left(X_{(m-1)ts}-L_n\right)\left(X_{mts}-L_n\right) < 0 \quad (1)$$

If this condition is satisfied, a level crossing (s_i) is detected in the interval ((m-1)ts, mts). The quantized value of the time interval ($Q(s_i)$) and the amplitude of the level crossing (λi) are recorded to give the sample set $\{Q(si),\lambda i\}$, as given in Eqs. (2) and (3)

$$Q(s_i) = (m-1)t_s + t_s/2 \quad (2)$$

$$\lambda_i = L_n \quad (3)$$

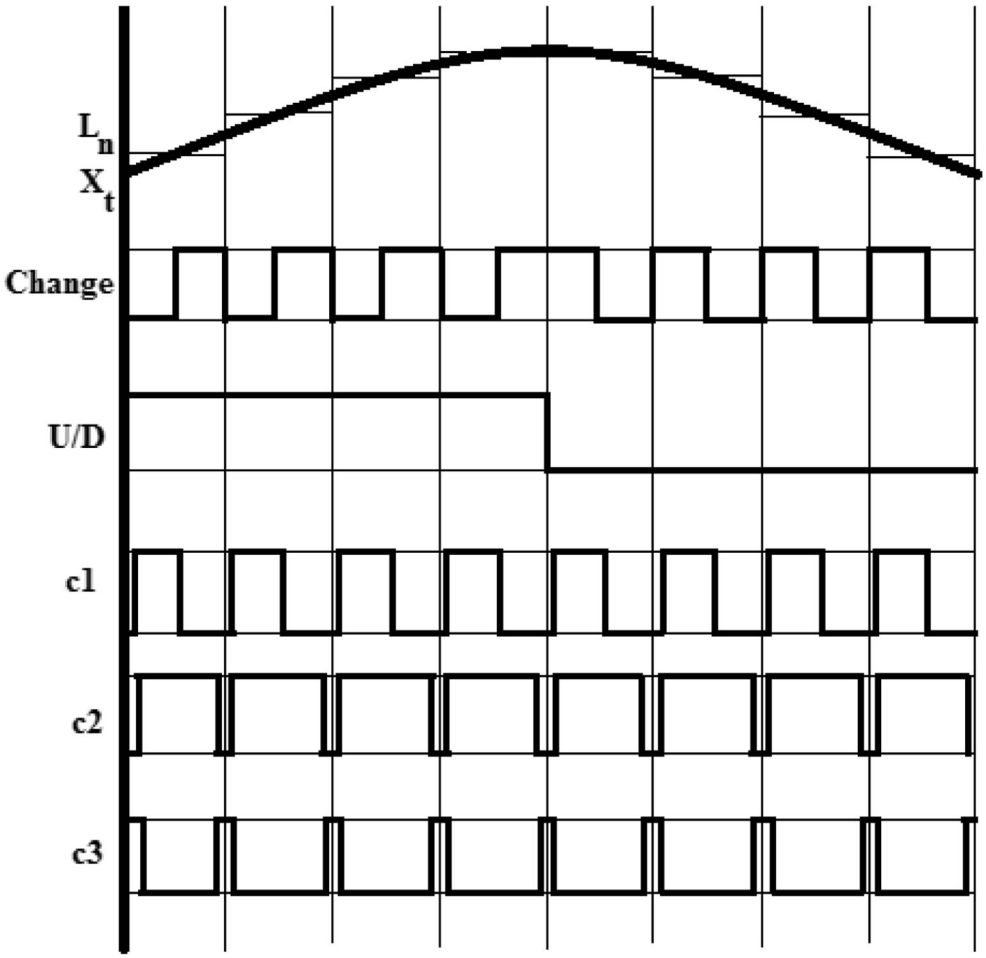


Fig. 7 Example waveforms and clocks for the circuitry

Above Eqs. (1), (2) and (3) holds true for every general LC ADC. The proposed algorithm aims at adaptively determining the threshold set L_n. The algorithm used for implementation of the proposed ADC is presented in Algorithm 1 as shown in Table 1. The sample set $\{Q(s_i), \lambda_i\}$ is used to obtain the reconstructed signal using polynomial interpolation.

Circuit implementation

The circuit implementation of the asynchronous adaptive threshold LC ADC consists of a main comparator, a threshold generating circuitry, an up or down signal generating circuitry, a counter and a timer. The structure of the proposed LC ADC

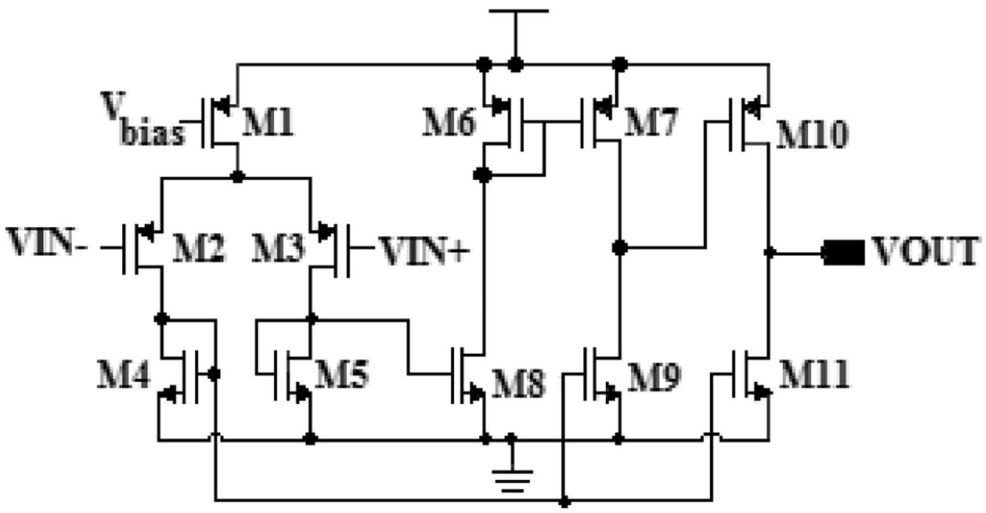


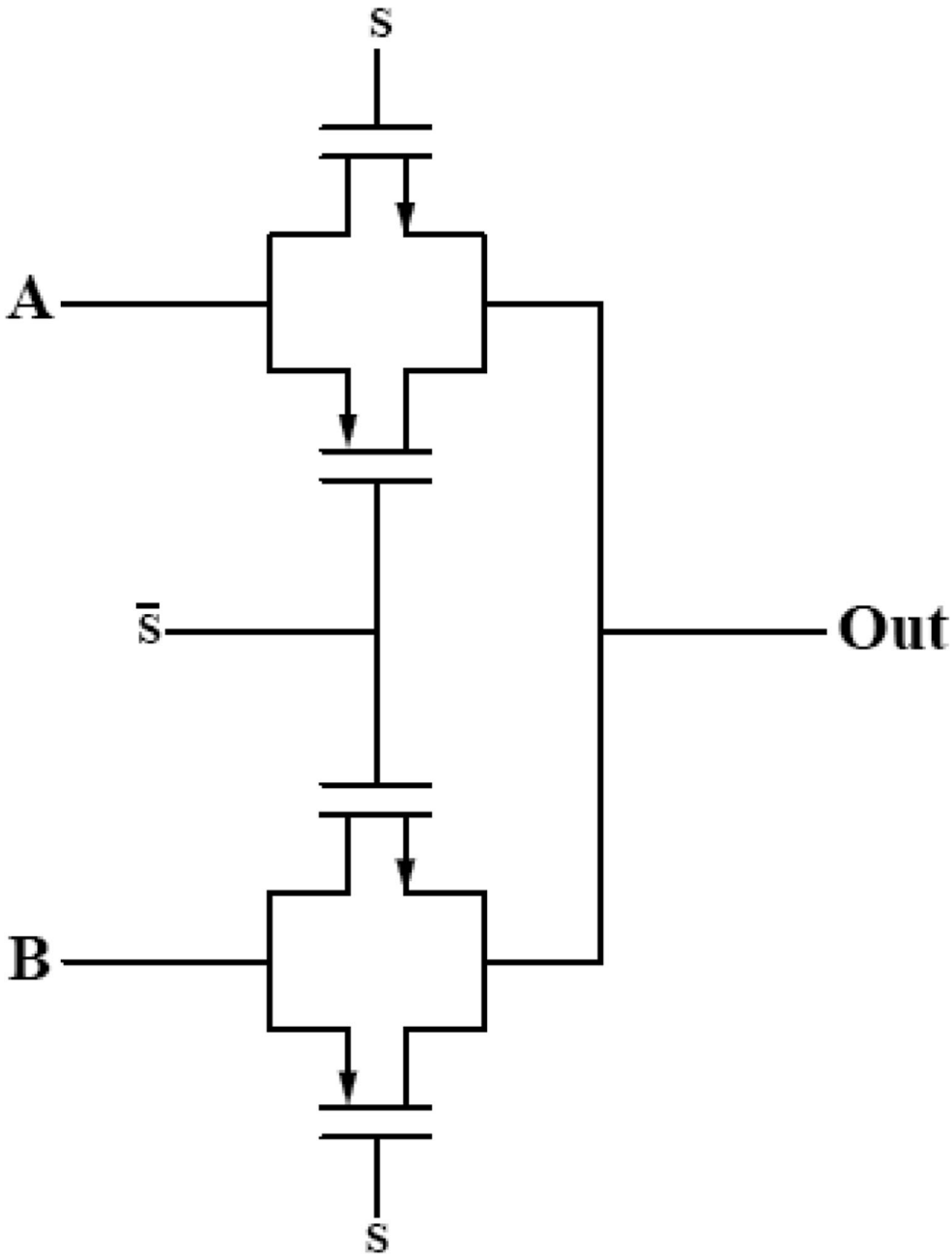
Fig. 8 Three stage continuous time input comparator

Table 2 Design parameters of the three stage continuous time input comparator

	W/L ratio
M1	10/2.5
M2,M3	10/0.4
M4-M11	2/0.4
V_{bias}	0.6 V
Supply voltage	0.8 V

is shown in Fig. 6. The input signal is given to the threshold generating circuitry which obtains the threshold by calculating the mean from the maximum and minimum of input signal for every v seconds. The generated threshold is compared with the delayed input signal in the main comparator to give change signal. The change signal gives the instants at which the input signal x_t crosses the threshold set L_n. The up/down digital logic generates the up or down signal to determine the varying directions of the input signal. The change signal is given as the clock for the up/ down counter and timer.

Fig. 9 Multiplexer



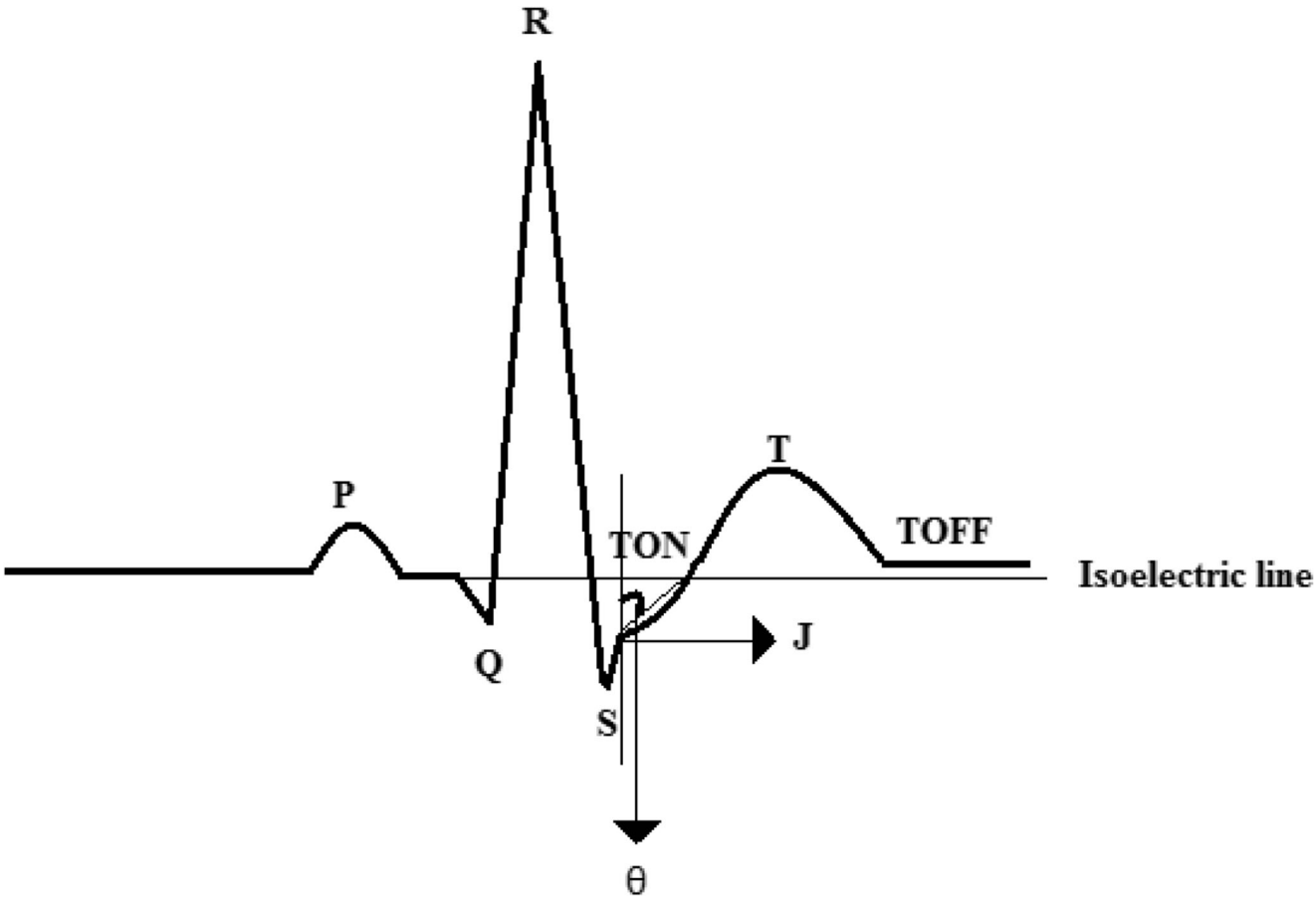


Fig. 10 Normal ECG signal

Example waveforms and clocks for the circuitry are shown in Fig. 7. In Fig. 7, for an input signal x_t to the system, a threshold set L_n is generated by the threshold generating circuitry. During the update interval of v seconds, 2 multiplexers namely mux1 and mux3 and a comparator com1 are used to find the maximum value of the input signal. For the update interval of v seconds, com1 compares the input signal with the output of the mux1 which is the maximum value from the previous comparison. When input signal is greater than the maximum value from the previous comparison, comparator gives high or low output. When clock c2 is high, mux3 forwards the output from the comparator to the mux1 which act as its select input. The mux1 forwards either the input signal or the maximum value from the previous comparison whichever

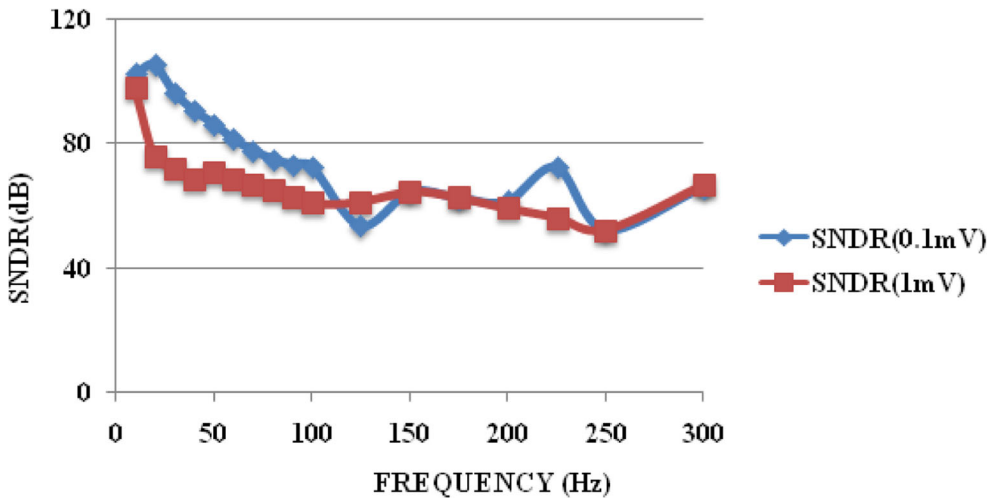


Fig. 11 SNDR for 0.1 mV and 1 mV input signals as a function of input frequency ranging from 0.01 Hz to 300 Hz

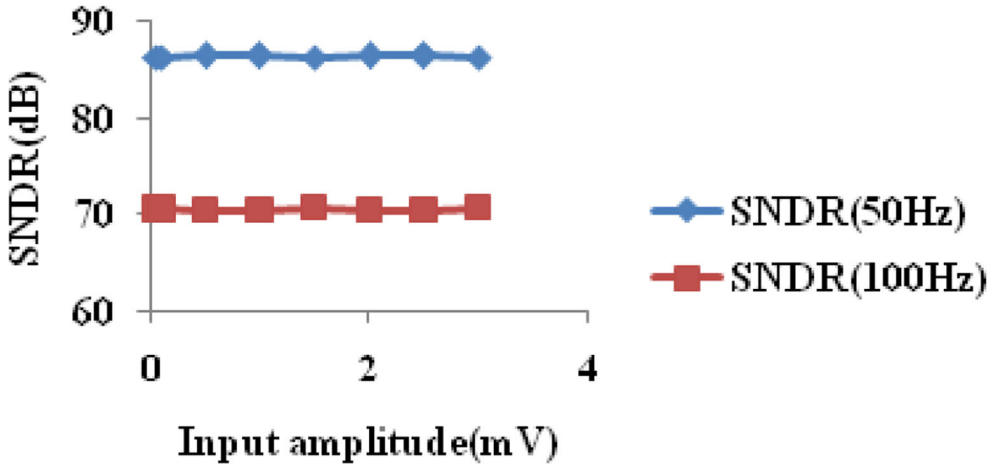


Fig. 12 SNDR for 50 Hz and 100 Hz input signals as a function of input amplitude ranging from 0.05 mV to 3 mV

is greater. When clock c2 is low at the end of the update interval, mux3 output retains the maximum value from the previous comparison. Similarly, Multiplexers namely mux4 and mux6 and a comparator com2 are used to find the minimum value of the input signal in the update interval of v seconds. When c3 is high at the end of the update interval, the switch c3 closes and forwards the maximum and minimum values in the update interval to mux2 and mux5 respectively. When c3 is low, the mux2 and mux5 retains the maximum and the minimum values from the previous update interval and the retained values are averaged to yield the threshold for the input signal.

Since threshold is from the previous update interval, the input signal needs to be synchronized with the threshold generated. So the input signal is delayed using ideal delay block in CADENCE analog library for simulation. The delay block was set to a sum of v seconds and an average delay caused by the threshold generating circuitry measured by simulation. Implementing the analog delay block in hardware can be quite challenging which is not within the scope of this paper. A wound coaxial wire can be used to implement the analog delay. But the wound coaxial wire occupies a large area. A CMOS bucket brigade device [21] with an analog integrated circuit can be used to implement the analog delay. A circular buffer [22] with lower resolution ADC and DAC can be also used to implement the required delay.

The delayed input signal is compared with the generated threshold using main comparator to give the change output. The change signal gives the instants at which the input signal x_t crosses the threshold set L_n. An edge triggered T flip-flop is used to generate the up/down signal using the clock c1. The up/down signal shows the varying direction of input signals. The change signal is given to the up/down counter. The up/down counter generates digital code representing amplitude information using the change signal. The timer gives time stamp information from the change signal. The conversions in the LC ADC architecture are driven by change signal and up/down signal which are derived from the input variations. Since the conversions are not triggered by any global clock, electromagnetic interference in the circuit is reduced drastically.

A three stage continuous time comparator with a PMOS input pair is used in this LC ADC as the main comparator and

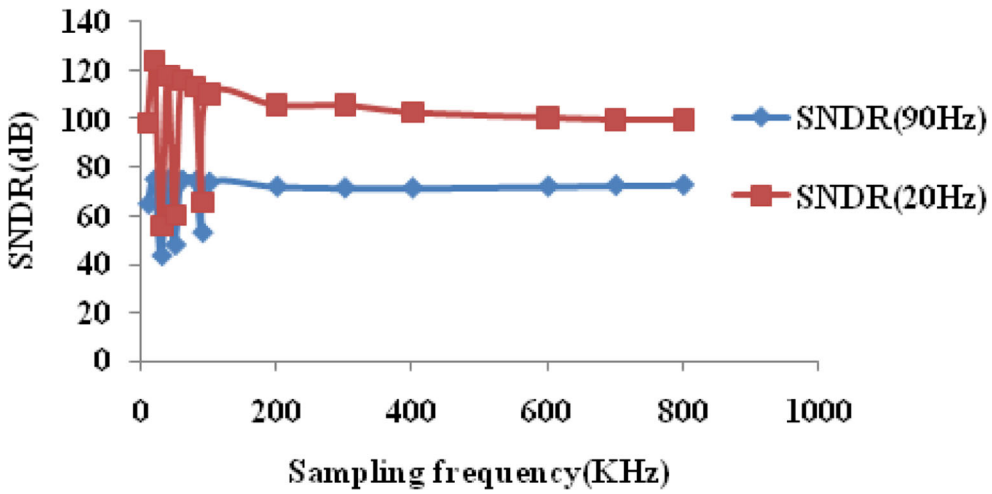


Fig. 13 SNDR as a function of the sampling rate for 20 Hz and 90 Hz sinusoidal input signal

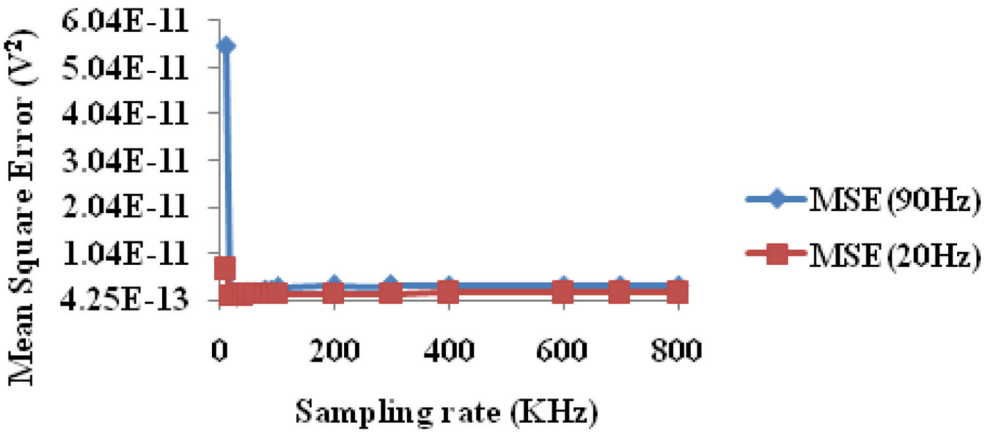


Fig. 14 Mean square error (MSE) as a function of the sampling rate for 20 Hz and 90 Hz sinusoidal input signals

in threshold generating circuitry. The circuit diagram of the three stage continuous time input comparator is shown in Fig. 8. All the MOSFETs in the three stage comparator are designed to operate in subthreshold region to lower the power consumption. The W/L ratios of the designed three stage comparator are shown in Table 2.

The multiplexer in LC ADC uses switches realized by NMOS and PMOS transistors connected in parallel as shown in Fig. 9. Small size transistors are chosen for the multiplexer to reduce the charge injection and clock feedthrough. Charge injection occurs when the transistor is turned off and channel charge is dispersed to the source and drain. The source which acts as the sampling capacitor experiences an error in the sampled voltage. The coupling due to gate source overlap capacitance also contributes to the total error voltage known as clock feedthrough. The switches in the threshold generating circuits are implemented using MOSFETS which are also made small. The averaging circuit is implemented using a

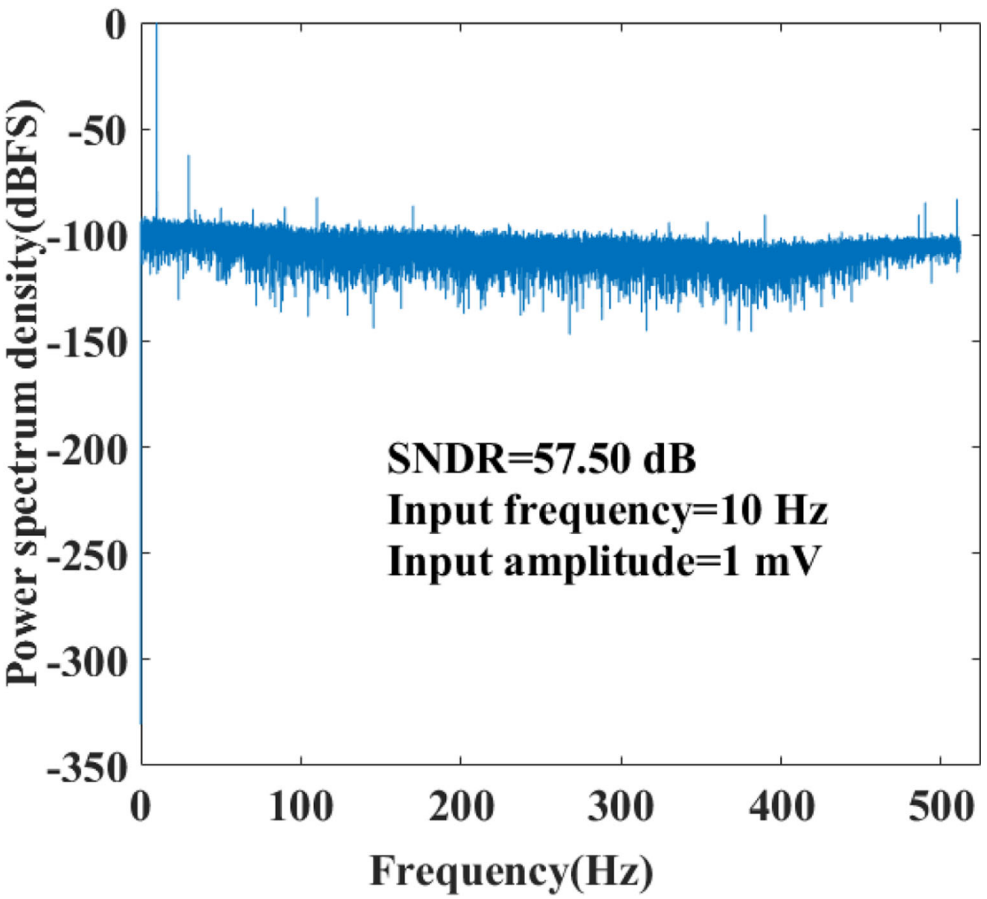


Fig. 15 FFT of the measured ADC Output

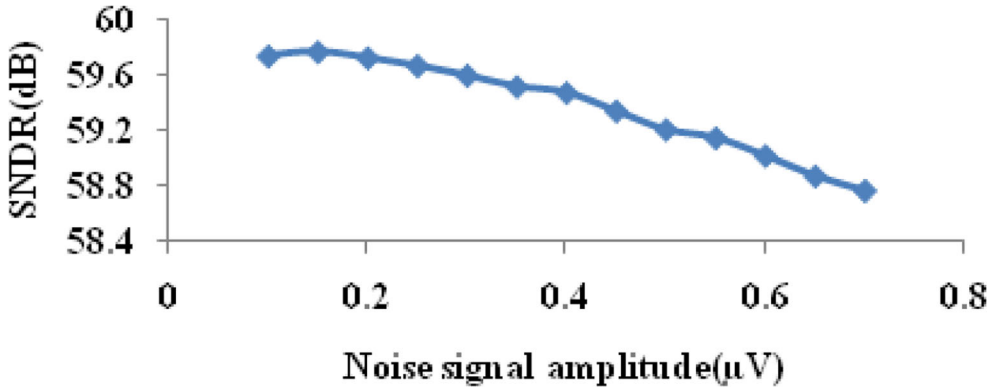


Fig. 16 SNDR of the LC ADC for a 50 Hz noise signal with varying amplitudes ranging from 0.1 μV to 0.7 μV

passive circuitry of 2 equal 1 K resistors. The LC ADC was implemented in CADENCE using 180 nm technology excluding the edge triggered T flip-flop, up/down counter and timer which were designed in MATLAB.

Feature extraction and diagnosis of abnormality from ECG

Electrocardiogram (ECG) is the recording of electrical activity of the heart. It is in the frequency range of 0.01 Hz to 300 Hz and the amplitude range of 0.05 mV to 3 mV. The wavelet transform based on daubechies wavelet (db4) [18] is used in this paper for feature extraction and detection of abnormalities in ECG. The reconstructed signal is decomposed into 4 levels using daubechies wavelet (db4). The features of ECG signal shown in Fig. 10 such as P wave, Q wave, R wave, S wave, J point, T wave, TON and TOFF are extracted from the decomposed ECG signal. The QRS complex of frequency 10 Hz and amplitude 1 mV constitutes the dominant wave of ECG signal. The RR interval is determined from the ECG signal to calculate the heart rate as given in Eq. 4.

$$\text{Heart rate} = 60/\text{RR interval in seconds} \tag{4}$$

When the heart rate is between 60 beats per minute (bpm) and 120 bpm, heart rate is normal. When the heart rate is lower than 60 bpm, arrhythmia bradycardia is diagnosed. When the heart rate is greater than 120 bpm, arrhythmia tachycardia is diagnosed.

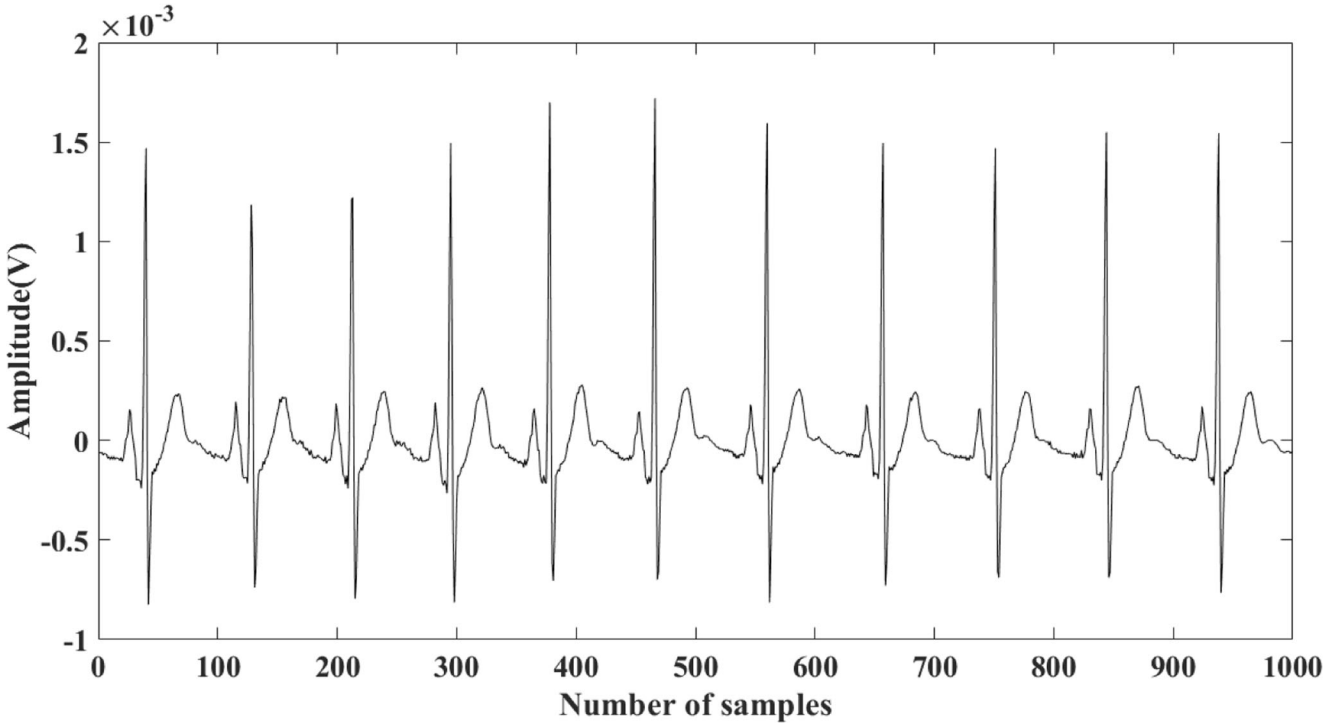


Fig. 17 Input ECG Signal

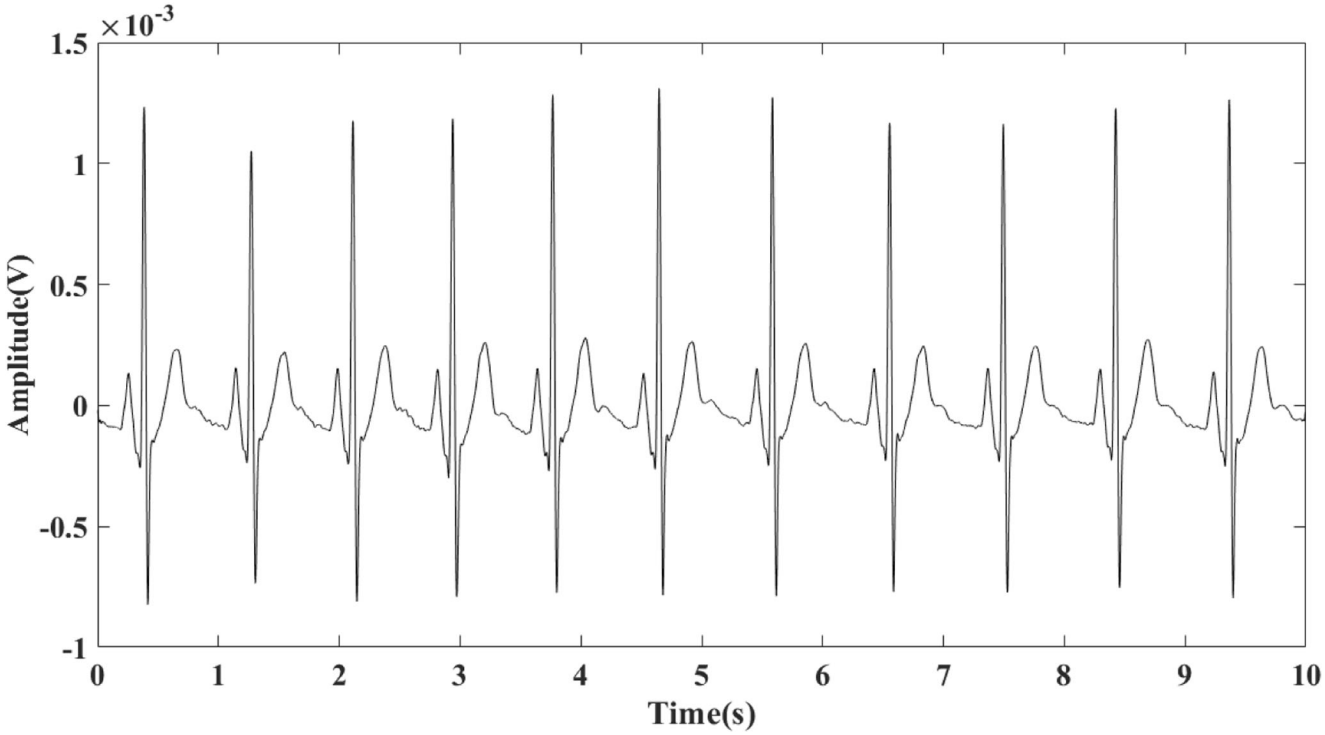


Fig. 18 Reconstructed ECG signal

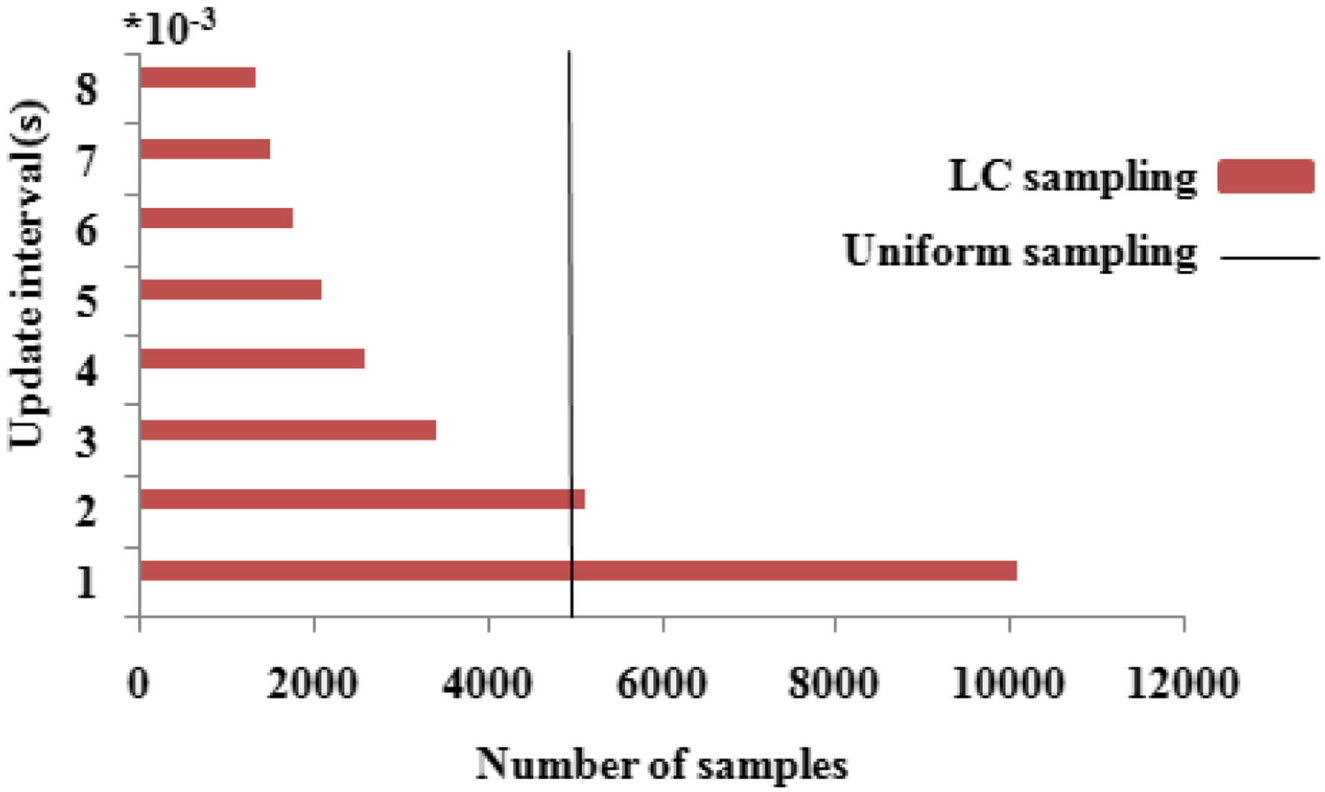


Fig. 19 Comparison between the number of samples generated by LC ADC and uniform sampling system

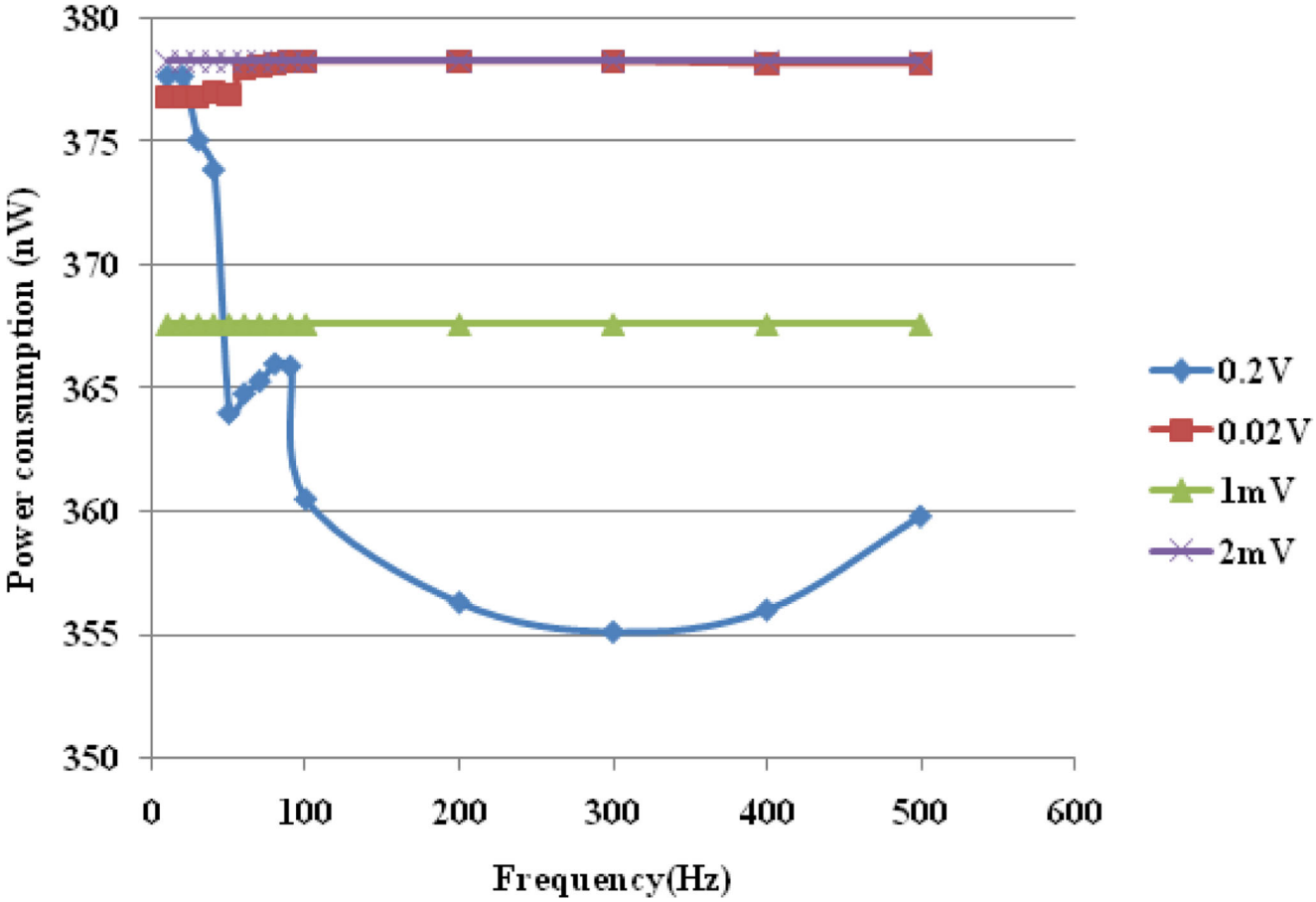


Fig. 20 The power consumption of LC ADC for different input amplitudes ranging from 0.2Vpp to 2mVpp at frequencies ranging from 10 Hz to 500 Hz

Results and discussion

The proposed LC ADC was implemented in MATLAB algorithmically. Figure 11 shows the SNDR of the ADC for 0.1 mV and 1 mV sinusoidal input signal as a function of input frequencies ranging from 0.01 to 300 Hz. The ADC algorithm was implemented in MATLAB to work at an update interval ranging from 0.4 ms to 0.05 ms and input sampling frequency of 200 KHz. The signal was reconstructed using 1024 points by polynomial interpolation. The order of the polynomial interpolation was varied from 3rd to 6th to find the best SNDR. The SNDR ranges from 105.5 dB to 52.2 dB as shown in Fig. 11. The SNDR of the proposed ADC decreases as the input frequency increases due to slope overload distortion. As the input frequency increases, the rapid change of input signal cannot be properly reconstructed by the designed LC ADC due to slope overload distortion. This is unlike the alias free LC ADCs [8, 19] whose SNDR increases as the input frequency increases. Figure 12 shows the SNDR for 50 Hz and 100 Hz input sinusoidal signals as a function of the input amplitude ranging from 0.05 mV to 3 mV at an update interval of 0.1 ms and input sampling frequency of 200 KHz. The Fig. 12 shows that the SNDR do not vary significantly with the amplitude. A plot of the measured SNDR of the LC ADC as a function of the sampling frequency for 20 Hz and 90 Hz, 0.1 mV input sinusoidal signal at an update interval of 0.1 ms is given in Fig. 13. The decrease in the SNDR at some sampling frequencies lower than nyquist frequency as shown in Fig. 13 is due to the occurrence of aliasing and harmonic distortion. The mean square error of the LC ADC is calculated from the square of difference between original signal and reconstructed signal. The mean square error as a function of the sampling rate at 90 Hz and 20 Hz for 0.1 mV input sinusoidal signal at an update interval of 0.1 ms is shown in Fig. 14. The signal is reconstructed using a third order polynomial interpolator for plotting Figs. 12, 13 and 14. The FFT of the ADC running at an update interval of 2 ms and a sampling frequency of 10 KHz for 10 Hz, 1 mV sinusoidal input signal reconstructed using 1024 points by third order polynomial interpolation is shown in Fig. 15. A SNDR of 57.50 dB, effective number of bits(ENOB) of 9 bits and a mean square error (MSE) measure of $1.368*10^{-8}$ V^2 was achieved by the proposed algorithm for 1 mV amplitude, 10 Hz input signal in MATLAB.

The SNDR of the LC ADC when implemented can be limited by the noise in the ECG signal. Mostly the sources of noise are power line interference, electrode contact noise, baseline drift and motion artifacts. The noise in the ECG

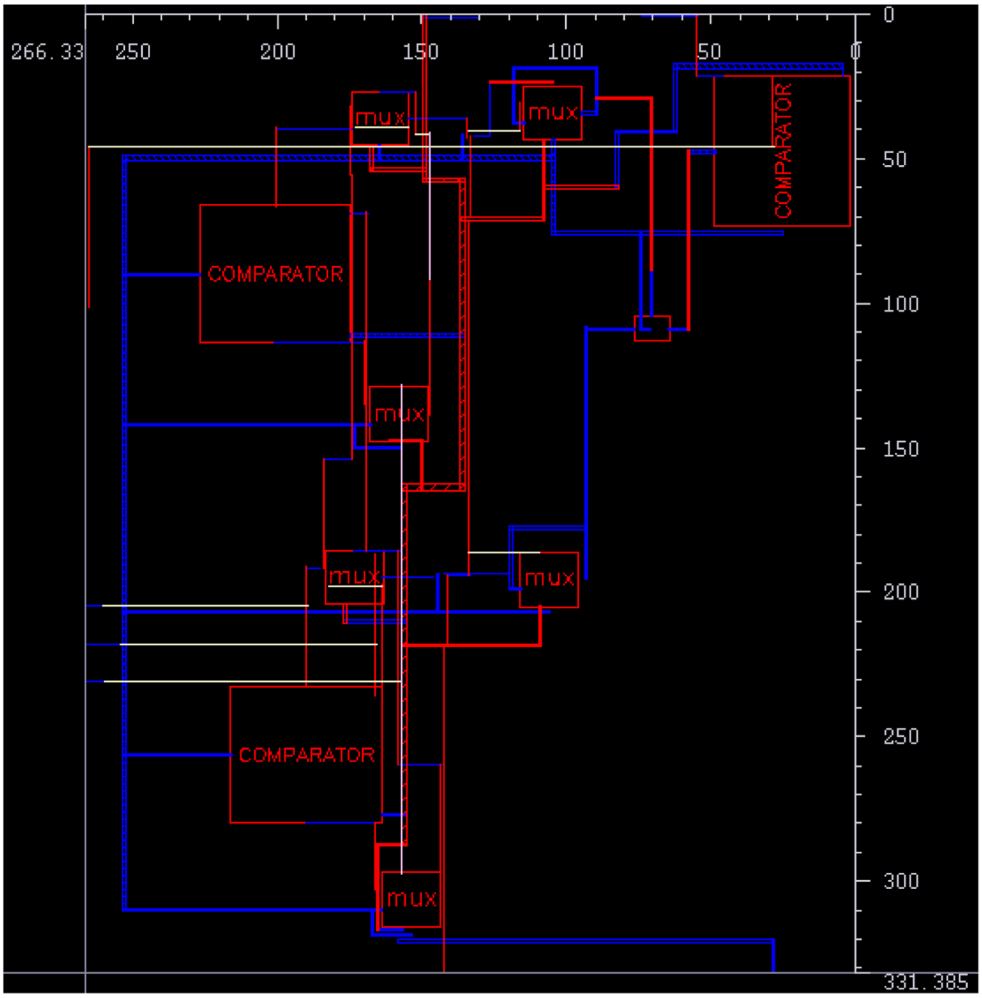


Fig. 21 Layout of LC ADC

signal can be reduced using filtering. The peak SNDR of the LC ADC can also be limited by the analog circuitry imperfectations below to that predicted by MATLAB simulations. The presence of spurious signals in generated threshold, imperfect comparator operations, flicker noise and thermal noise can also introduce errors.

The peak SNDR in the MATLAB simulations can be achieved by keeping the noise introduced by analog circuitry much less than the total allowable noise. The total allowable noise, N_{tot} of the LC ADC can be calculated using

$$A_{rms} = A_P/2\sqrt{2} \tag{5}$$

$$SNDR = 20\log_{10}\left(A_{rms}/N_{tot}\right) \tag{6}$$

Where Ap is chosen as 1 mV which is the amplitude of the dominant wave QRS complex. A_{rms} is calculated to be around $3.5355*10^{-4}$ V. To achieve the SNDR around 56 dB for a 10 Hz input ECG signal, N_{tot} should not exceed 0.472 μV. Figure 16 gives the SNDR of the LC ADC simulated with 50 Hz noise signal with varying amplitude added to the 1 mV, 10 Hz sinusoidal input in MATLAB. The LC ADC is made to run at an update interval of 2 ms and a sampling frequency of 10 KHz.

The quantization error in a sample arises from either the uncertainty in the quantization levels or the finite resolution in time [1]. The quantization error due to the uncertainty in determining the quantization levels is reduced by the adaptive determining of the threshold in the proposed technique. The RMS quantization error due to time uncertainty for a sinusoidal signal of given amplitude is proportional to the inverse of clock oversampling ratio, i.e., the ratio of the timer frequency to the input signal frequency.

The record a01 from the Apnea-ECG database in physionet for 10 s shown in Fig. 17 is used as input signal to LC ADC. The LC ADC operates at a sampling frequency of 10 KHz with an update interval of 2 ms. The reconstructed input ECG signal from LC ADC using polynomial interpolation is shown in Fig. 18. LC ADC is considered as a promising alternative to the uniform sampling system since it produces fewer numbers

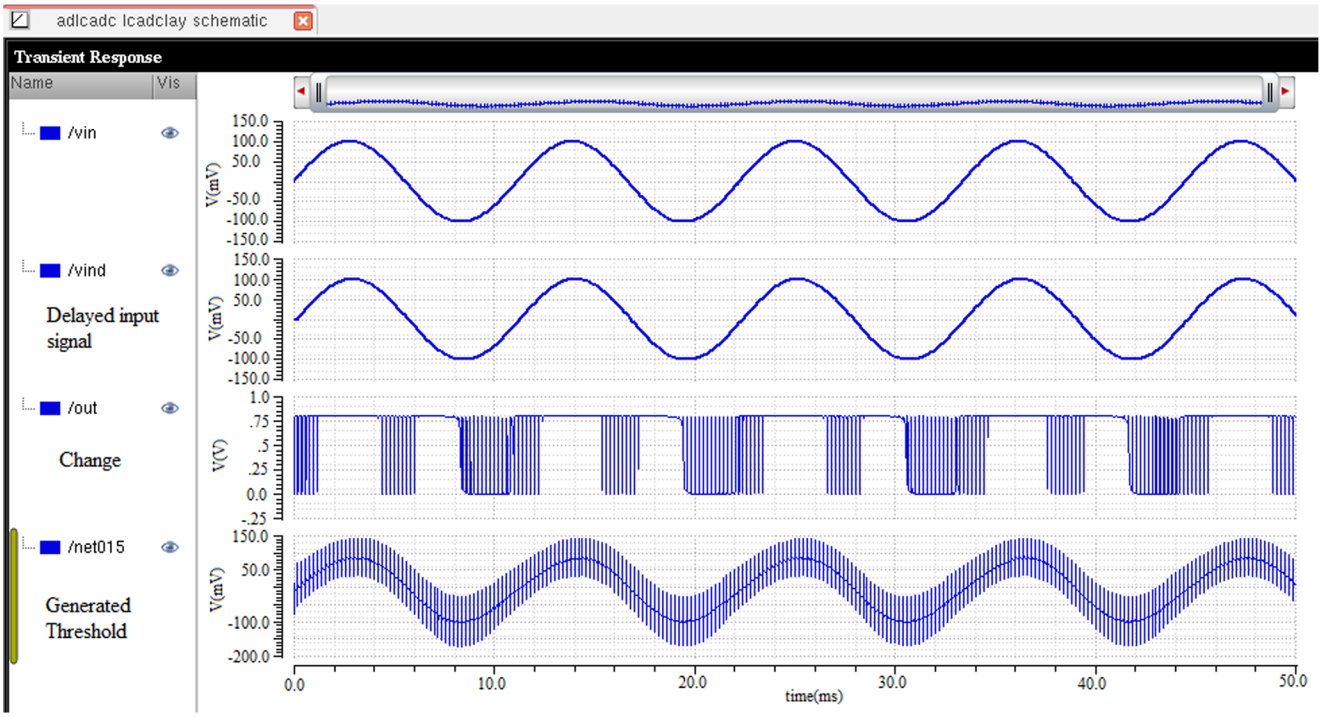


Fig. 22 The waveforms from post layout simulation of LC ADC in CADENCE virtuoso

of samples. Samples are constantly generated in a uniform sampling system whereas LC ADC generates samples only when the input signal crosses the threshold level. Figure 19 compares the number of samples generated by the LC ADC and uniform sampling system for the input ECG signal shown in Fig. 17. The LC ADC operates at a sampling frequency of 10 KHz with varying update interval. Uniform sampling system operates at 500 Hz which is the general operating frequency range for a long term ECG monitoring system. Figure 19 shows that LC ADC generates a lower number of samples as the update interval increases.

The LC ADC excluding the up/down digital circuitry, counter and timer was implemented in CADENCE virtuoso using 180 nm technology. Figure 20 shows the power

Table 3 Comparison of the simulated results of designed LC ADC with previous LC ADC architectures ([a]without counter and timer, [b]without T flipflop in up/down circuitry, counter and timer)

Performance metrics	[2]	[3]	[5]	[7]	[20]	This work
Technology	180 nm (Nanosim and HSpice)	0.35 µm (CADENCE and MATLAB)	MATLAB simulation	MATLAB simulation	180 nm (CADENCE and VERILOGA)	180 nm (CADENCE AND MATLAB)
Reconstruction	–	ACT algorithm	6th order polynomial interpolation	–	3rd order polynomial interpolator	3rd to 6th order interpolation in MATLAB
Input bandwidth	1KHz-5 MHz	1-10 MHz	9.42KHz	20-200hZ	5KHz	5 Hz–3.3KHz
Power consumption	34.4 µW-437.81 µW	175 mW	–	–	1.42µW[a]	367.6nW[b]
Area(mm^2)	–	1.8	–	–	–	0.088
Supply voltage(V)	–	3.3 V	–	–	0.7 V	0.8 V
Input voltage(V)	–	10 mV-1.65 V	Varies	–	0.8 Vpp	1mVpp
SNDR (dB)	–	75	84.5 dB peak	–	47 dB	57.50–98.8
MSE (V^2)	–	–	–	7*10^-4	–	1.368*10^-8

Table 4 Comparison of the threshold determining techniques in previous LC ADC architectures with the proposed adaptive threshold asynchronous ADC

LC ADC architectures	Description	Advantages	Disadvantages
[2–5]	-Generated using resistive or capacitive divider network	-Less design complexity	-Optimal placement of levels cannot be guaranteed resulting in information loss
[6, 8]	-Adaptive threshold -The feedback n- bit DAC loop generates an input compatible thresh old voltage from the digital output	-Threshold was determined exploiting the statistical properties of the sparse signal reducing the information loss	-To ensure proper correction of the reference level, the input signal must not cross any quantization level until the ADC is ready to treat another data causing a \delay. -Occurrence of glitches -Stability issues of the feedback loop
[9]	-Off-chip fixed reference levels generated using potentiometer -The feedback 1 bit DAC loop forces input to stay in the comparison window.	-Less design complexity -Feedback loop ensures that reference levels stays within the input range reducing the information loss	-Offset of the comparators cause inaccuracy in comparison levels resulting in quantization error -Feedback loop introduces stability issues in the circuitry
[7]	-Sequential algorithms that randomly select level set at fixed intervals from a class of possible level sets according to a Probability Mass Function generated by each class of input.	-Optimal placement of levels within the dynamic range of input signal -No feedback DAC loop	-Only algorithmic simulations are performed with no circuit design provided.
This work	-Sequential algorithm that generate threshold for a fixed interval (v seconds) from the mean of maximum and minimum of input signal in the fixed interval	-Optimal placement of levels within the dynamic range of input signal reducing information loss -No feedback DAC loop	-A delay of v seconds occurs in generating the digital output -Spurious signals in generated threshold

consumption of LC ADC excluding the up/down digital circuitry, counter and timer for different amplitudes ranging from 0.2 V to 2 mV for various frequencies. The LC ADC occupies an area of 266.33*331.385 μm^2 as shown in the layout of LC ADC generated using CADENCE virtuoso in Fig. 21. The waveforms from the transient analysis of post layout simulation in CADENCE virtuoso for 1 mV, 90 Hz input signal is shown in Fig. 22. Figure 22 shows presence of spurious signals in the generated threshold from the threshold generation circuitry which is given as the input to the main comparator. This occurs due to the charge injection and clock feedthrough in the switches and multiplexers of threshold generating circuitry. The generated threshold and the delayed input signal is given as input to the main comparator which generates the change output. The post layout simulation of the LC ADC circuitry consumes an average power of 367.6 nW for 1 mVpp, 90 Hz input sinusoidal signal which is same as in pre-layout simulation. This shows that parasitic capacitance and resistance in layout do not have much effect on the working of LC ADC. The simulated results of the LC ADC are compared with simulated results in previously published LC ADC architectures in Table 3 showing superior results. The proposed LC ADC achieves low power and area compared to other ADC architectures as inferred from Table 3. Previous literature shows LC ADCS using resistive or capacitive ladder network as in uniform sampling, feedback DAC and sequential algorithms to generate the required threshold as explained in Table 4. Advantages and disadvantages of the threshold determining techniques in previous LC ADC architectures are compared with the proposed adaptive threshold generation technique in Table 4.

Table 5 R-R interval, heart rate, and detection of abnormality from the ECG signal

Record 232			Record 201		
RR interval Extracted(s)	Heart rate extracted (bpm)	Heart rhythm abnormality	RR interval Extracted(s)	Heart rate extracted(bpm)	Heart rhythm abnormality
1.4721	40.76	bradycardia	0.4677	128.27	Tachycardia
0.7359	81.53	normal	0.7680	78.13	Normal
0.7904	75.91	normal	0.8118	73.91	Normal
1.9742	30.39	bradycardia	0.6518	92.06	Normal
0.7320	81.97	normal	0.8594	69.81	Normal
0.7651	78.4	normal	0.6921	86.69	Normal

The efficiency of the asynchronous adaptive threshold ADC in ECG signal processing is tested by applying wavelet transform to the reconstructed signal and extracting the features of the ECG signal like P wave, Q wave, R wave, S wave, J point, T wave, TON and TOFF. Table 5 shows the RR interval, the heart rate and heart rhythm abnormality obtained using wavelet transform from the reconstructed ECG signal. Input ECG signal used is record 232 and 201 from the MIT-BIH Arrhythmia database in physionet for 6.819 s.

Conclusion and future work

The implementation of asynchronous adaptive threshold LC ADC is presented in this paper. An algorithm for asynchronous adaptive threshold LC ADC is proposed and implemented using MATLAB. The algorithm designed a LC ADC of high SNDR and few samples. The peak SNDR simulated can be achieved practically by keeping the noise introduced by analog circuitry much less than total allowable noise. The algorithm implemented using 180 nm technology in CADENCE operates at a low supply voltage, and achieves lower power and area making it suitable for wearable devices. Comparison of the simulated results of this work with simulated results of Li & Serjdin, 2012 [20] shows a 74% decrease in power consumption. Also comparison of the proposed LC ADC with Kozmin et al., 2009 [3] shows a 95% decrease in area. The LC ADC also works on a low supply voltage of 0.8 V. We show case studies of RR interval, heart rate and heart rhythm abnormality detection using the proposed asynchronous adaptive threshold LC ADC to prove the functionality of the design.

This paper presents only the simulated results of the asynchronous threshold LC ADC. Future work will focus on the fabrication of the chip. Implementing analog delay in hardware is quite challenging. A bucket brigade device using MOSFETs [21] or wound wire or circular buffer [22] can be used for delaying the ECG signal which comes under the future scope of this work. The spurious signal in the generated threshold should also be reduced to achieve a more efficient reconstruction of the input signal.

Funding This research received no external funding.

Compliance with Ethical Standards

Conflicts of Interest The authors declare no conflict of interest.

References

1. Sayiner, N., Sorensen, H. V., and Viswanathan, T. R., A level-crossing sampling scheme for A/D conversion. IEEE Transactions on Circuits and Systems II: Analog Digital Signal Processing 43(4): 335–339, 1996. https://doi.org/10.1109/82.488288.
2. Akopyan, F., Manohar, R., Apsel, A. B., A level-crossing flash asynchronous analog-to-digital converter. Proceedings of the IEEE International Symposium on Asynchronous Circuits and Systems, Berkeley, 11–22, 2006. doi: https://doi.org/10.1109/ASYNC.2006.5
3. Kozmin, K., Johansson, J., and Delsing, J., Level-crossing ADC performance evaluation toward ultrasound application. IEEE Transactions on Circuits and Systems I: Regular Papers 56(8): 1708–1719, 2009. https://doi.org/10.1109/TCSI.2008.2010094.
4. Mark, J. W., and Todd, T. D., A nonuniform sampling approach to data compression. IEEE Transactions on Communications 29(1): 24–32, 1981. https://doi.org/10.1109/TCOM.1981.1094872.
5. Wang, T., Wang, D., Hurst, P. J., Levy, B. C., and Lewis, S. H., A level crossing analog-to-digital converter with triangular dither. IEEE Transactions on Circuits System I, Regular Papers 56(9): 2089–2099, 2009. https://doi.org/10.1109/TCSI.2008.2011586.
6. Allier, E., Sicard, G., Fesquet, L., and Renaudin, M., Asynchronous level crossing analog to digital converters. Elsevier Measurement Journal 37(4):296–309, 2005. https://doi.org/10.1016/j.measurement.2005.03.002.
7. Guan, K. M., Kozat, S. S., and Singer, A. C., Adaptive reference levels in a level crossing analog-to-digital converter. EURASIP Journal on Advances in Signal Processing 2008(1):1–11, 2008. https://doi.org/10.1155/2008/513706.
8. Schell, B., and Tsividis, Y., A continuous-time ADC/DSP/DAC system with no clock and with activity-dependent power dissipation. IEEE Journal of Solid-State Circuits 43(4):2472–2481, 2008. https://doi.org/10.1109/JSSC.2008.2005456.
9. Li, Y., Zhao, D., and Serjdin, W. A., A sub-microwatt asynchronous level-crossing ADC for biomedical applications. IEEE Transaction on biomedical circuits and systems 7(2):149–157, 2013. https://doi.org/10.1109/TBCAS.2013.2254484.
10. Inose, H., Aoki, T., and Watanabe, K., Asynchronous delta-modulation system. Electron Letters 2(3):95–96, 1966. https://doi.org/10.1049/el:19660077.
11. Kozat, S. S., Guan, K. M., and Singer, A. C., Tracking the best level set in a level-crossing analog-to-digital converter. Digital Signal Processing 23(1):478–487, 2012. https://doi.org/10.1016/j.dsp.2012.07.018.
12. Canal, M. R., Comparison of wavelet and short time Fourier transform methods in the analysis of EMG signals. Journal of Medical Systems 34(1):91–94, 2010. https://doi.org/10.1007/s10916-008-9219-8.
13. Ubeyli, E. D., Cvetkovic, D., and Cosic, I. J., AR spectral analysis technique for human PPG, ECG and EEG signals. Journal of Medical Systems 32(3):201–206, 2008. https://doi.org/10.1007/s10916-007-9123-7.
14. Belkheiri, M., Douidi, Z., Belkheiri, A., ECG beats extraction and classification using radial basis function neural networks. In S M., Kumar, S., (Eds.), *Proceedings of the Fourth International Conference on Signal and Image Processing 2012 (ICSIP 2012)*, *Lecture Notes Electr. Eng.* 2:127–136, 2012. doi: https://doi.org/10.1007/978-81-322-1000-9_12
15. Stamkopoulos, T., Maglaveras, N., Diamantaras, K., and Strintzis, M., ECG analysis using nonlinear PCA neural networks for ischemia detection. IEEE Transactions on Signal Processing 46(11): 3058–3067, 1998. https://doi.org/10.1109/78.726818.
16. Li, Y., Mansano, A. L., Yuan, Y., Zhao, D., and Serjdin, W. A., An ECG recording front end with continuous-time level-crossing

sampling. IEEE Transaction on biomedical circuits and systems 8(5):1932–4545, 2014. https://doi.org/10.1109/TBCAS.2014.2359183.

17. Mansano, A. L., Li, Y., Bagga, S., and Serjdin, W. A., An autonomous wireless sensor node with asynchronous ECG monitoring in 0.18μm CMOS. IEEE Transaction on biomedical circuits and systems 10(3): 602–611, 2016. https://doi.org/10.1109/TBCAS.2015.2495272.
18. Gneecchi, J. A. G., Magaña, R. M., Espinoza, D. L., Anguiano, A. D. C. T., Archundia, E. R., Patiño, A. M., and Miranda, R. C., DSP-based arrhythmia classification using wavelet transform and probabilistic neural network. Biomedical Signal Processing and Control 32:44–56, 2017. https://doi.org/10.1016/j.bspc.2016.10.005.
19. Weltin-Wu, C., Tsividis, Y., An event-driven, alias-free ADC with signal-dependent resolution. *Proceedings of IEEE Symposium on VLSI Technology and Circuits*, Honolulu, HI, USA, 2012, 28–29, 2012. doi: https://doi.org/10.1109/VLSIC.2012.6243773
20. Li, Y., Serdijn, W. A., A continuous-time level-crossing ADC with 1-bit DAC and 3-input comparator. *IEEE International Symposium on Circuits and Systems*, Seoul, Korea, 1311–1314, 2012. doi: https://doi.org/10.1109/ISCAS.2012.6271481
21. Ushiyama, O., Okajima, H., Sasaki, Y., and Hasegawa, M., Noninvasive recording of his bundle activity with an analog delay device in normal subjects and patients with atrioventricular block. Hearts and Vessels 10(5):241–248, 1995. https://doi.org/10.1007/BF01744903.
22. Smith, S. W., Digital signal processors. *The scientist and Engineer's Guide to*. Digital Signal Processing 28:506–509, 2002 Retrieved from www.dspguide.com.