IMAGE & SIGNAL PROCESSING

Design and Implementation of Low Power High-Efficient Transceiver for Body Channel Communications

S. Vijayalakshmi[1] (ID) · V. Nagarajan[1]

Abstract

Body channel communications (BCC) have been researched while an allowing technology to improve necessities for the low power and high reconfiguration power in wireless telemetry systems used at wireless communication purpose. Conventional features on BCC are concentrated mostly on modeling of channels by using of an efficient measurement technique, wireless transceiver design and then by means of a transmission technique. Particularly, the wireless digital transmitting, developed as a personalized method intended for the body channel, offers wanted to develop flexible and low power BCC systems. With the developing level of wearable communication protocol and applications, there may be an increasingly reliable on an adaptable BCC transmitter that helps both data reconfigure power and power reduction condition. In this paper, an extremely reconfigurable Hamming Encoding Digital Transmitter (HEDT) which works with both reconfigurable data and power reduction condition that supports from two innovative operation conditions is suggested. In a HEDT device, the overall data rate is controlled by the level of Hamming codes designed to make use of in the perfect BCC band of 20–100 MHz. The proposed Hamming Encoded Transmission method achieves seven times improved data rate when compared with conventional BCC processors. The next unique implementation technique is based on the usage of Frequency Shift Keying (FSK) of a Hamming encoded HEDT approach. This approach permits the BCC transceiver to use the perfect channel with bandwidth among 40–100 MHz. Thereby half the clock rate reduces 40% of overall power utilization. The HEDT system is completely designed in a 65 nm CMOS procedure. It uses a primary area of 0.14×0.2 mm. When functioning below a data-rate of 60 Mb/s (low power) condition, the BCC transmitter utilizes only 1.00 mW.

Introduction

Latest technical advances of body built-in sensors can produce a recognition of wise microsystems is a combination of various sensors and transmission handling circuitries. This must be a substantial influence on an assortment of a programmed device such as for example telemetry systems, automatic gadgets, environmental parameters monitoring systems and telemetry diagnosis systems [1–4]. Such schemes must have several characteristics, for example, cost-effective, real and robustness-timely data handling. Sensor technology takes part Radio Frequency schemes in the similar field because of their data detecting properties. The wireless data communication system is a practical and cost-effective approach for transferring digital data over long-range distances, under noisy channel conditions. Various medical technologies have already been designed for a variety of body implanted medical uses [4–6]. An overall system diagram of a wireless medical data sensing program is shown in Fig. 1.

It includes analog signal stage, in which the analog sensors are used for sensing the analog signals. In the binary data stream, a digital transceiver chip device and RF device are used. The RF device is a combination of both digital
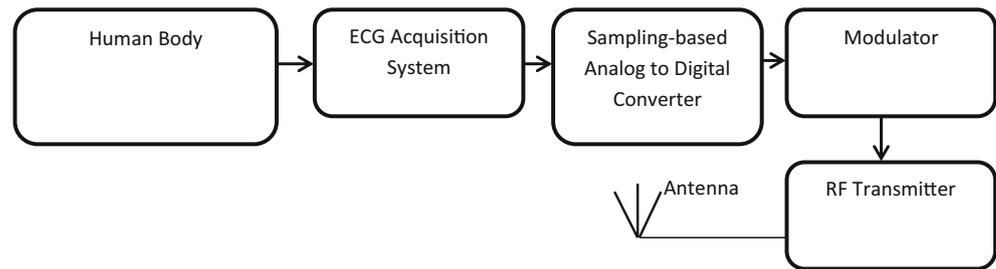
✉ S. Vijayalakshmi
   sankarviji7@gmail.com

   V. Nagarajan
   nagarajanece31@gmail.com

[1] Department of Electronics and Communication Engineering, Adhiparasakthi Engineering College, Melmaruvathur, Tamilnadu, India

Fig. 1 Block diagram of BCC-based wearable ECG

transmitter and receiver. In the binary data stream, the analog signals are encoded into digital. For designing this overall system, Tanner EDA simulator is used. By this simulator various circuit design methodology is utilized. With the help of a variety of mathematical data combination methodologies, different combinations of blocking networks are prepared prior to the transceiver design. One appealing specification may be the cap power to cluster connected blocks and group organized to create a single check. The overall circuit offers all specifications of the first blocks. These specifications are characterized on display in a far more modest system. In this proposed paper, an ECG data sensing transceiver has been designed, tested and then simulated. ECG sensors data signals used for transceiver overall performance calculation while they need a substantial part in telemetry monitoring and disease diagnosing system [6–10]. The innovation in this function is found with Tanner EDA simulator to create a very accurate whole circuit prototypical for a biomedical device that's integrating some true data indicators to get reliable performance outcomes. Many Hamming procedures have already launched in the machine to accomplish high-speed digital data compression.

The frame work of this research paper is sectioned below. Section 2 gives the introduction to Body Channel Communications. Section 3 describes briefly about the system design of proposed HEDT for BCC systems. Section 4 discuss about the result analysis. Section 5 concludes with the conclusion.

Body channel communications

Body channel Communications (BCC) was proposed by Zimmerman despite the fact that a novel discussion technology to boost data among digital sensor systems in Wireless Body Area Network (WBAN). Both transmitter and receiver are making use of antennas.

BCC is done through the human body, which acts as a transmitting medium for coupling frequency signal. The transmitter modulates the encoded data for transmitting in the wireless channel. The transmitter's software coded program is not directly associated with the data, but it is related to the power consumed by the devices which work on the data. Also for

configuring and making a setup, a radio interconnection is necessary. For modulating a base band signal on to the carrier frequency there is an inherent limit of power utilization. Compare to BCC, the radio frequency communication has a path fading effect because of many systems such as medium, refraction, diffraction and absorption of data rate are involved. The behavior of users are get constrained by cables which possess a tendency to be tangled. [11–16].

Wireless devices should have its available power resource to utilize and a radio frequency consumes much more potential to transmit and also should have the reality [17]. Unlike wired and wireless communication strategies, BCC features on the RF transmitting channel, a physical Layer (PHY) for WBAN systems gives been standardized by just the IEEE 802. Correctly, therefore, such Radio Resource of recurrence frequency coupling can be executed since the particular body comprises many cells having an increased dielectric regular. In the IEEE prevalent, the complete information is transmitted through the body. The transmitted information is passed over the selected regular domain which is having digital codes band devoid of an uninterrupted degree of repetition frequency modulation. For shorter range of communications, BCC definitely comes as a scheme within the characteristic. Also it offers an excellent intuitive assistance, whenever a challenging process of a network produce isn't needed [18–22].

Proposed HEDT design for BCC systems

The wearable body sensing devices which regularly collect analog data from a person or mature individuals are focused on a few essential indicators such as for example pulse, heart rate, EMG waves, blood pulse rate, mind signals, etc.

The primary top features of the wireless microsystem will later make use of a Multisensory array, analog data transmission signal conditioning circuits, an electronic signal processor chip, a radio transmitter, and a power resource (battery) (Fig. 2). Because of this system, both analog signal conditioning circuits and an electronic signal processor have been applied by means of designing an application-specific integrated circuit (ASIC) silicon chip.

This segment describes our proposed Radio Frequency (RF) type BCC processor offered with an efficient telemetry

Fig. 2 Diagram of the proposed overall BCC transceiver
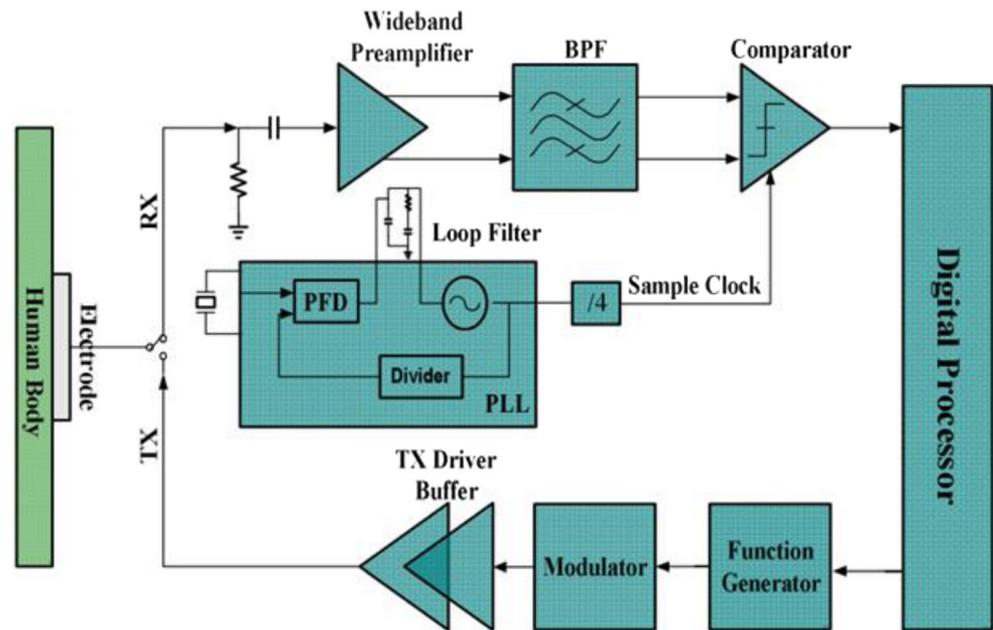
ECG sensing transmitter for transferring the ECG data. The RF type BCC processor determines the actual essential data signals transmitted in assessment to conventionally accessible RF- ECG to display the utility and strength of it. While comparing with the previous ECG BCC system, the designed BCC-based ECG transmitter avoids any type of wires and the disturbances of day to day activities. Figure 2 shows the overall design of BCC-based telemetry ECG, which we proposed. It contains an ECG signal detector device with 2 data acquiring electrodes and one number of ground sensor electrodes. Also it has an ADC converter which transforms the time-varying ECG analog signals into digital bit processing configuration. The BCC transceiver transfers the digital ECG data for the purpose of using BCC methodology. It is usually described as a health-inspecting device that can be connected on top of left side pectoral area through the calculation of ECG data signals.

At the first step, several ECG analog data acquired from the body are brought in and then encoded into a digital signal. Electrode sensors are used to analyse the electric activity of the ECG data signals in patient's heart. The acquired ECG signal is analog data of center analog signal activity of the patient is usually a mixture of sound waves and random data waves. The ECG transmission comes with an amplitude level differ from 0.1–5 mV with an implied value of 3.0 mV as demonstrated through Fig. 2. It was found that the mean power ratio of the related peak rate of repetition frequency was to be 0.10–180 Hz. The noisy section of the waveform signifies the breathing object which is a quite frustrating problem because its frequency is quite near to the true ECG data signal. ECG waveforms in the individual heart had a sinusoidal waveform of the signal; therefore the digital data could be

encoded short of valuable digital pulses chain. The arriving analog data signals get converted into digital signals effectively with the selection of 10 ms as sampling time. It is also mentioned that the ratio of variation of the analog data could be very dissimilar. The automatic machine functions could be split into 4 primary steps.

The outcome of the initial step is an electronically encoded data bits utilizing a Hamming process, which is termed within the following segment. The ECG digital data from the different stations are handled simply with the Digital Processor device, which symbolizes the next step. The digital data via to each wireless digital channel is framed, next multiplexed by mux circuit and then compressed with the compressor at this time before that data is fed into the RF unit. In this point of time, the digital serial data become transformed with frequency shift keying and delivered through a noisy wireless Radio Frequency transceiver. In the receiver section, the digital serial data is demodulated. The overall result outcomes of the designed transceiver system shall be measured in two steps. The first step is that the result of digital data compression is executed by the Processor device and then verified with various Hamming encoding procedures. Hence, the RF channel parameters result for a particular selection of frequencies which are inspected for variable circumstances.

The Electrocardiography data signals can be sensed by the 2 numbers of data acquiring electrodes placed on our patient body, and then it is progressed into the ECG data sensor. In the ECG signal recognition unit, the ECG signal sensor includes a low pass filtration system, next band pass filter (BPF), and then finally differential operational amplifiers. Subsequently, almost all of the essential ECG signals happen to be focused below the frequencies in the order of 120 Hz. The two LPFs
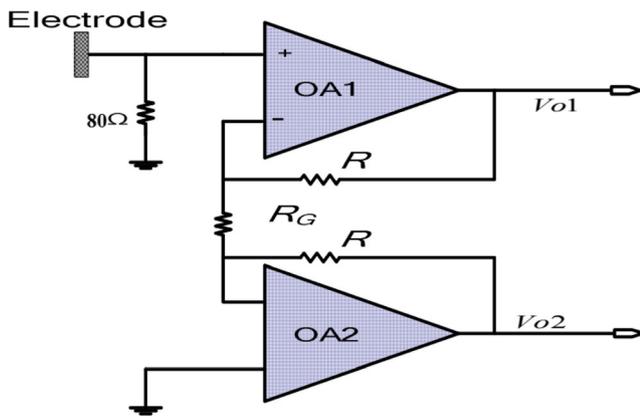
Fig. 3 Circuit of preamplifier circuits

up to recurrence frequency of 120 Hz are recycled correspondingly to get the ECG data signals under 120 Hz, additionally to filter the high range frequency signal noise interference from BCC indicators. To efficiently avoid the incursion of drift sound coordinates, high pass filter systems having a stop band frequency of 20 Hz are being used. For removal of unwanted authority frequency noise, BPFs with 40/80 Hz are being used. A good differential voltage amplifier with the intensification aspect of 60 dB is used to improve the feedback impedance. Then the ECG data indicators coming out from amplifier are fed into analog to digital converter. The digitized ECG signals coming out from ADC are delivered to the BCC processor for data transmitting purpose. The ADC with a sampling capacity of cutoff frequency 600 Hz, quantization degree of 8 bits data and amplitude 3 V is chosen to sample the ECG analog data indicators output.

For BCC process, the human body acts as a medium to work as band pass filter (BPF) system, which passes the signal bandwidth W is reliant upon the space in the middle of the transmitter and then the receiver electrodes. Also with a collection space between electrodes is 10 cm, if digital binary data is usually straight placed on the human skins, the

transmission of the wireless channel displays very thin number of small pulse without DC offset. Preamplifier framework is shown in Fig. 3.

$$A_V = (2R + R_G)/R_G = 1 + (2R/R_G) \qquad (1)$$

Analog Operational amplifiers OpAmp1 (OA1) and OpAmp2 (OA2) are mutually worked together to provide a reliable differential output along with a superior common mode rejection ratio (CMRR). The combination of resistors R and RG provides R = 60 k, OpAmp1 and OpAmp2 talk about the similar framework and usages.

To be able to understand a great similarity with the communication line model of patient body channel, we put in the 80 Ω resistor type. A device increase bandwidth of 1000 MHz was achieved by usage of feed forward procedure. With reference to Fig. 4, the proposed op-amp shown in the differential preamplifier runs on the dual step scheme to retain sufficiently large gain despite having a resistive type of load.

The band pass filtration (BPF) system, demonstrated in Fig. 5, can merely eliminate undesirable transmission. The BPF circuit supplies anti-aliasing procedure just before giving the signal to the comparator circuit. Filtering required bandwidth selection process is managed by the flexible integrator and capacitor array. By using the 4 bit digital data code and capacitor and resistor arrays, gain and predominant data of the given filtering frequency are achieved.

As the data rate of communication devices increases consistently through the years, the conversion rate of ADCs in these systems needs to increase. During the last decades communication devices have evolved a lot. Either through higher speed or more data capacity, constant technological improvements allow for new and better communication companies. Since at present data is processed digitally both ahead of and following its analog propagation, Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC)

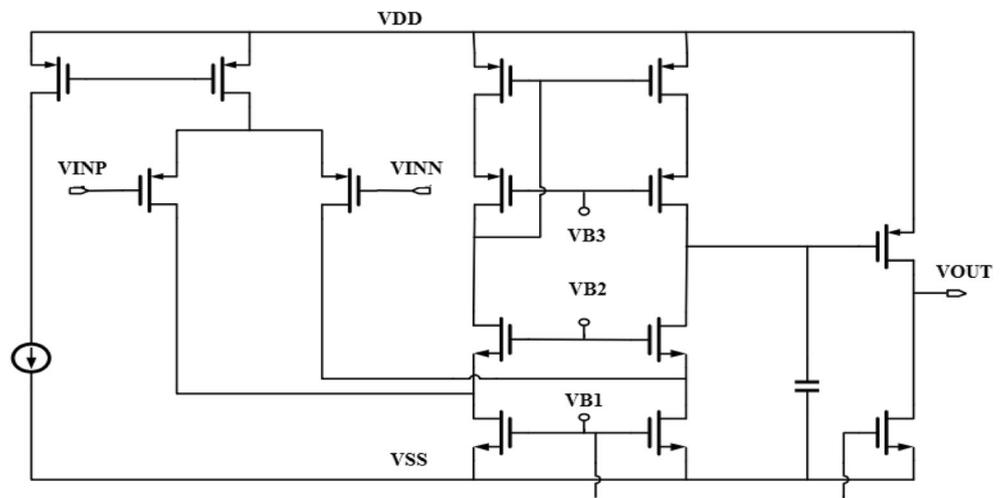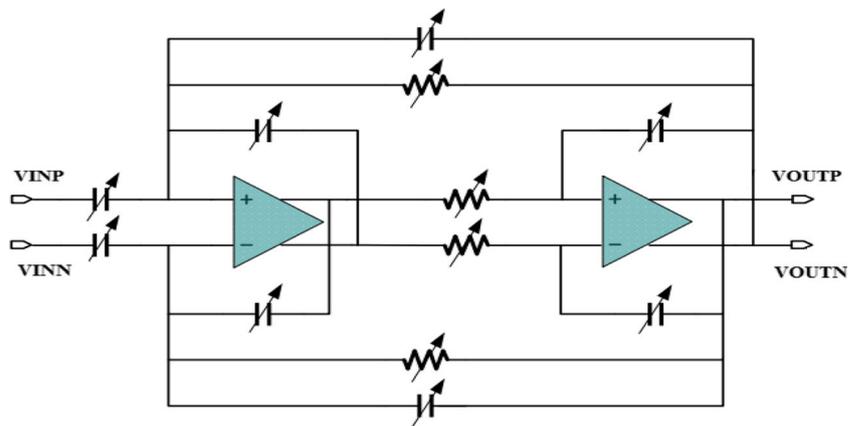**Fig. 4** Proposed preamplifier circuit

Fig. 5 Circuit diagram of band pass filter

are always necessary. Due to this fact, the regular evolution of communication technologies is possibly the biggest determination for ADC effectiveness rise, although ADCs are used in other types of systems (e.g., audio, video, instrumentation).

Performance increases in Digital-to-Analog Converters (DAC) are also highly motivated by communication systems since this digital processing is created before transmission. High enough sampling frequency could be obtained by time-interleaving multiple ADC stations. However, performance is bound by mismatches between the different channels. To guarantee the time-interleaved ADC's appropriate performance, a calibration system is generally designed to find and correct these errors.
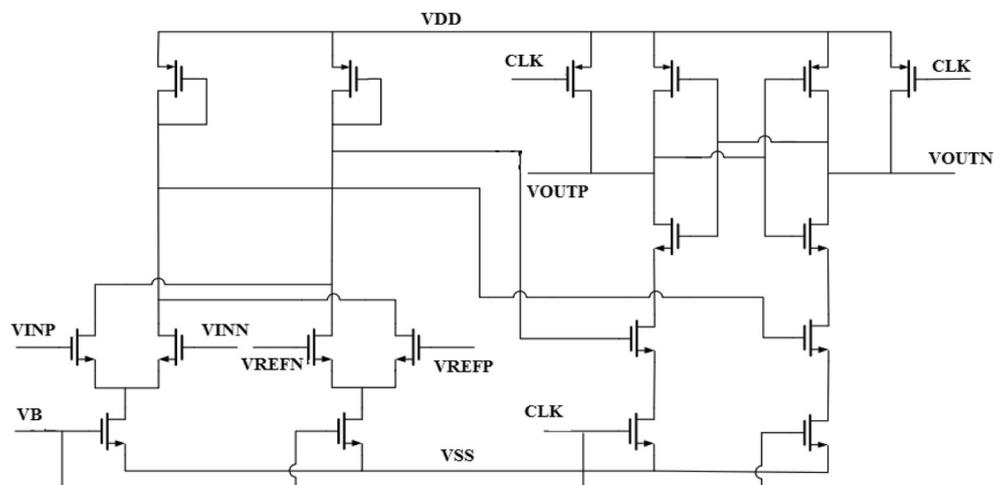
In Fig. 6, the SAR-ADC main block, its overall performance and its connected design difficulties are detailed and shown. Because of the reduced inherent gain of transistors within sophisticated CMOS process nodes, the multi-level amplifiers with many phases are gathering recognition within mixed-signal products. A brief discussion about the multi-level amplifier's rate of repetition frequency compensation is usually enclosed.

In body channel communications (BCC), the information are synchronously, that is, a group of digital binary data

transmissions over an individual human body are received by a receiver without any associated clock. By just suppressing the clock, a tidy clock is suppressed from the group of binary digital data and synchronizes the information. Because the transceiver works at bandwidth limited properties and at low recovered binary data rates, for instance, inter symbol interference or simply amplitude error source clock regularity counterweight among a transmitter and an excellent receiver are in fact allowable within the BCC transceiver. Hence, it is more essential for the Encoder circuit to come quickly to become concentrated on less power utilization rather than the high speed data procedure. However, under the situation of $V_{thn} + |V_{thp}| > 1$ V, the dissipation of energy in processor digital circuitry is normally proportional to the square of the base voltage. Appropriately, the processor includes Quadratic Digital sampling encoder design predicated on a low power DCO which is shown in Fig. 7.

To reduce the more power usage and more difficulty, the proposed low power Quadratic Digital Sampling circuit uses a 4-little bit UP/DOWN counter, a lock-state processor and a low voltage digitally controlled oscillator (DCO) along with a voltage reference. By using through the lock-stage brand and the 4-tad UP/Direct DOWN counter, the 4-little bit ECG

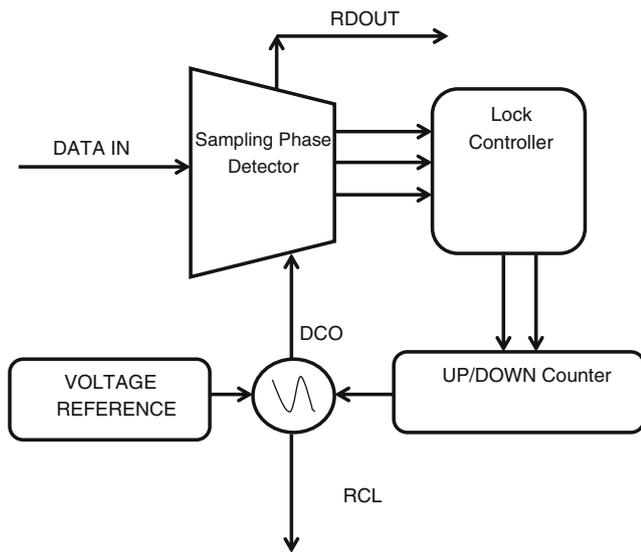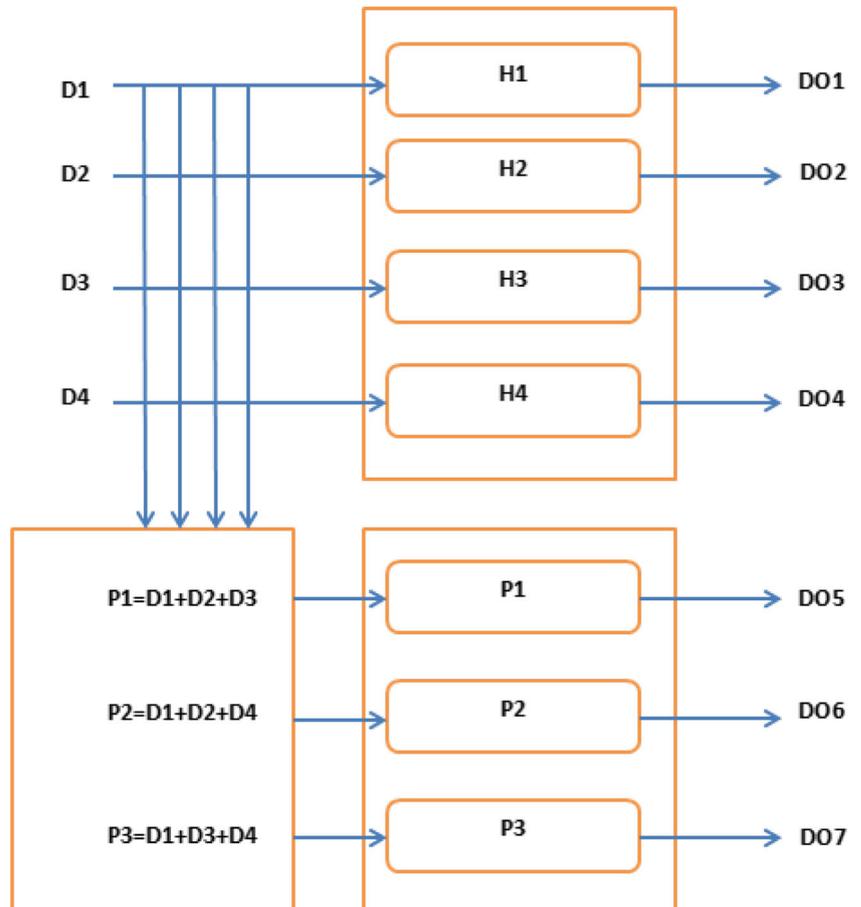**Fig. 6** Proposed low power SAR ADC

Fig. 7 Proposed low power quadratic digital sampling circuit

Then the measured 4-bit ECG digital data was given as input for the digital hamming data bit encoding circuitry. This suggested hamming encoder used to make the parity bit calculation for encoding 4-bit ECG data from the ECG Sensor. The encoded 7-bit ECG data can be considered using the next formula.
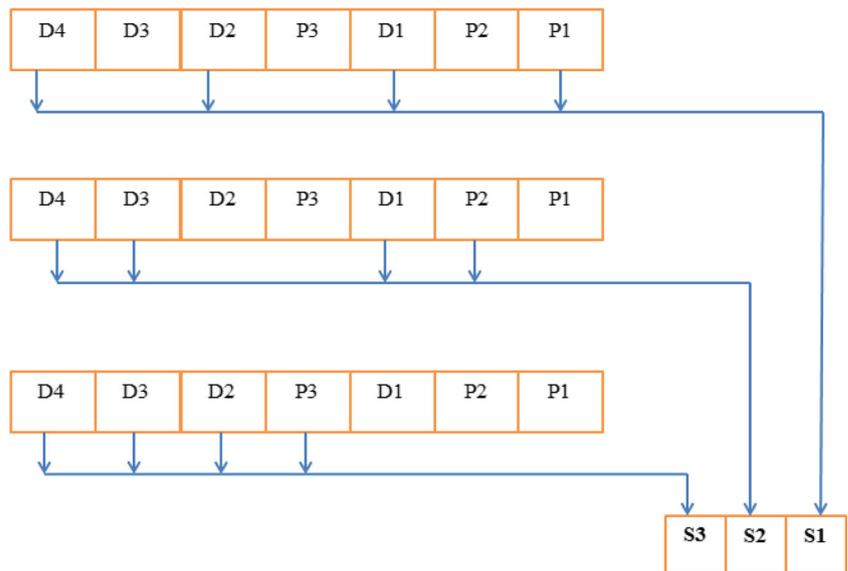
$$N+M+1 \leq 2P \tag{2}$$

N   means the Data Bit length,
M   means size of Input data
P   means parity bit numbers.

For the suggested encoder design it is to calculate 3 numbers of parity data bits predicated on the Hamming calculation method. The specific suggested hamming structured encoder circuit for BCC transmitter is displayed in the following Fig. 8.

Hamming data encoder

In Hamming BCC Design, The ECG digital data as input bits and the corresponding 3 parity data bits are deliberated using the below conditions.

indicators could be made by averaging and low move filtering the sampled ideals. Loop will get locked when the LC transmitting goes large. To generate 16 multi-stage clock indicators for quadratic sampling, the DCO managed by ECG (3:0) was created. Hence further reduction of power usage is achieved.

Fig. 8 Proposed hamming data encoder

Fig. 9 Design of hamming decoder for BCC

Parity1 = Data1 ⊕ Data2 ⊕ Data3
Parity2 = Data1 ⊕ Data2 ⊕ Data4
Parity3 = Data1 ⊕ Data3 ⊕ Data4.

On the Basis of information sent to the hamming encoder the 3 parity data bits are deliberate using the source ECG signals. The parity bits are put into the ECG signal and changed into the 7-bit ECG digital signals as shown in Fig. 8. Then the digital signals shall evaluate the determination of Decoder Procedure. The BCC Processor is achieving all operations of the communication procedure. Hamming ECG data decoding procedure is completed by the next process. Figure 9 shows the significance of the suggested hamming information decoder design. It employs for producing the decoding ECG data based on the Transmitter circuit output data. These Decoded data bits support the ECG Information from the Transmitter. Here data from the Transmitter resulting chances of error because of channel conditions. When we

apply D1 as an input to H1 we get the output as DO1. Similarly when we apply D2 as an input to H2 we get the output as DO2 like so on. An error within the Data1 generates the error in every three parity data bits. Error in Data2 will generate a conceivable error in P1 and P2. Error in the Data3 will outcome error in the P1 and P3. Finally, Error in Data4 will outcome error in the P2 and P3. After getting the ECG signals from the Hamming decoder the BCC transmitter will automatically correct the errors by inverting the error bit. Finally, it provides the benefits of error analysis.

The RF wireless devices are certainly admiring devices which are emerging to use all the way over even short distances. RF lines provide the selection of high speed data transfer in the order of Mbps at very low power. RF lines used for low capacity users who are properly speed. Within the past long time applications driven by info, very short range equipment found to be included in the range of 10–100 m. There are four trends are used for energetic growth of RF wireless communication in general.

1. To raise the cellular data potential demands in lightweight devices with greater bandwidth at less expensive electricity utilization.
2. To develop interior wireless communication along with abundant transmission frequencies.
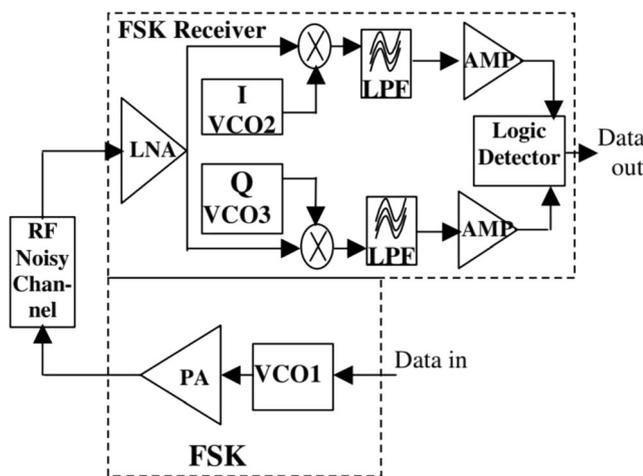

Fig. 10 The overall architecture of the digital FSK transmitter/receiver

Table 1 Power consumption comparison with conventional system

Transceiver Design	Dynamic Power(W)	Saving %	Total Test Power	Saving %
[4]	0.222	–	0.402	–
[11]	0.199	10.36	0.378	5.97
Proposed	0.100	16.00	0.2500	10.00

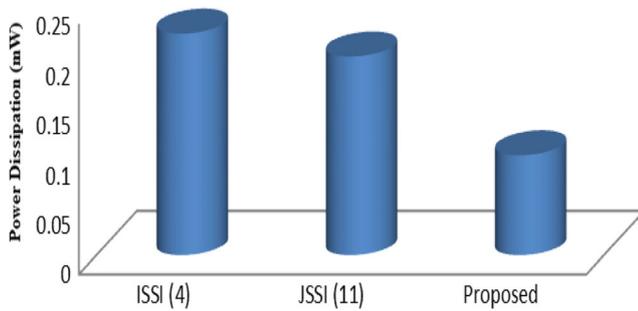Fig. 11 Variation of power dissipation with different technique

Fig. 12 Variation of fault coverage ratio with different technique

3. To decrease the semiconductor cost.
4. To reduce power absorption for signal processing.

Theoretically the cellular transmitters and receivers shall be divided into baseband and RF section. The collection of frequencies over which transmitters consider their incoming may be known as baseband. The receivers used to help to make their outcome. The function of the transmitter's RF portion is to convert the arranged baseband signal up to the chosen channel and to insert the same signal into the medium. A good transmitter has to transmit exact capacity of power by consuming a small amount of power as much as possible. A good receiver has to authentically recover tiny indicators while rejecting interferences away from the preferred channel.

RF systems are consisting of major blocks such as amplifiers, filters, mixers and oscillators. Here in this research work two important RF receiver architectures namely Heterodyne receiver and direct transformation architecture are considered. The Heterodyne receiver performs the following functions:

1. Converts the digital indicators to intermediate repetition frequency (IF)
2. Performs band-maneuver filtering and amplification
3. Translates the spectrum never to as much frequency once again.

The Direct-transformation is the second type in which the noise interference is reduced to zero rate of repetition.

Direct-transformation architecture is proved by means of the following two positive aspects while comparing to heterodyne receiver:

1. There will be no reliance on noises rejection filtration system because the intermediate regularity should come to be zero.
2. The IF filtration and further below conversion levels are replaced with LPF and baseband amplifiers which will be agreeable to monolithic integration.

Frequency Shift Keying (FSK) modulator is designed and integrated with Tanner EDA as shown in Fig. 10. In the indicated design, to derive from 0 and 1's through a bit stream with specific facts, a uniform random info generator is used. The voltage controlled oscillator (VCO) approaching voltage can be varied to ±0.5 instead rather than 0 or 1. That is integrated to really have the same regularity transformation for both tones by multiplying quantity of sensitivity of the VCO and this value. The power amplifier (PA) is a non linear unit which reveals a superior 60% efficiency for powerful modulation techniques as the FSK [11]. The FSK waveforms have not any sudden modification stage, but exhibiting a long-term packet. This means that FSK signals possibly get amplified by using non-linear PA's without spectral re-escalation.

The low noise amplifier (LNA) stands for the original receiver gain stage as well as noise amount is put into that of the machine. Within LNA, it is necessary to model transmitting non-linearity, saturation, two types of sounds (white colored and flicker), compression and slew charge limiting. The outcome from the LNA is blended with two quadrature oscillators that produce reliability add all the insight carrier charge of repetition. For alternative to both stations, two low pass filtration systems (LPF) with razor sharp cut-off features are used. A Butterworth analog filtration system is chosen for both these units.

This block possesses crucial influence on the machine efficiency. The main function of these devices is to extract the bad symbols of the implication signal which has a logic system. As a combinational logic system approach, the incoming indicators from both quadrature channels are examined as above. The outcome tad worth is extracted in the incredibly best stage by using SR flip-flop.

Result analyses

The complete outcomes of the proposed Low Power BCC Transceiver Design are defined below. The Hamming and

Table 2 Comparison for BER coverage with conventional system

Transceiver Design	Average BER Covered (100 Packet Sent Operations)	Error Coverage Ratio
[4]	80	80%
[11]	85	85%
Proposed HEDT System	99	99%

Device Utilization Summary (estimated values)				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	
Number of Slices	19	768	2%	
Number of Slice Flip Flops	7	1536	0%	
Number of 4 input LUTs	35	1536	2%	
Number of bonded IOBs	3	63	4%	
Number of GCLKs	1	8	12%	

Fig. 13 Proposed BCC design area utilization

RF Transmitter based Proposed Processor designed and verified by using Tanner EDA. The results of the proposed HEDT scheme clearly implies that the suggested Hamming established BCC Transceiver Design is having better Data processing rate and operating power compare to the capacitive coupling schemes.

The Table 1 and Fig. 11 demonstrate the power consumption of numerous BCC Transceiver Design with reference to the Proposed Processor Design. While specifying the Table 1 we can find that the Frequency sampling activity does a significant role in the Transceiver design. The HEDT Transceiver Design reduces power consumption for screening power and achieves an improved BER.

In essence, in the Transceiver scheme, practically 80% of errors participate in the noisy channels and packet processing Errors. Assume Qs denote that standard quantity of packets sent functions applied to find the random packet errors and Qr denotes that the common number of packet receiving process required for finding the random bit problems. The complete error coverage of proposed design comparing with the conventional systems is described in Table 2.

The Table 2 and Fig. 12 obviously describes the suggested Hamming based BCC Transceiver Design having the improved BER coverage ratio with reference to the usual BCC Transceiver Models.

The Fig. 13 displays that the average area used by the proposed BCC Transceiver Design. The HEDT area used by the HEDT system is surprisingly low when compared to the traditional Transceiver Designs. As well, this factor brings about less power consumption.

In Table 3, the most modern digital data transmission schemes are compared considering the proposed transceiver,

optimum data amount, 3 dB bandwidth related to transmit spectral mask (TSM) and fc. In general, the FSDT is standardized as BCC Transmitter in the IEEE requirements 802.15.6 for WBAN.

Based on the carrier frequency of the transmit scheme with the proposed transceiver, the association of the latest data transmission methods are shown in Fig. 14.

The overall performances of BER are demonstrated in Fig. 15. There is absolutely no performance reduction between the standard condition and the reduced power condition even though the transmission power efficiency for the reduced power operation condition is lesser than that of the regular condition. In the reduced power operation condition, the transmission power efficiency is insignificant as the next most main frequency of the Hamming data codes is usually in the perfect transmission band rather than the dominant important frequency.

Based on the data rate of the transmit scheme with the proposed transceiver, Fig. 16 displays the association of the most recent data transmission methods. The proposed hamming based scheme has better data rate compare to conventional schemes.

Nevertheless, in the reduced power condition, the clock frequency is reduced to 100 MHz, which resulted in data-rate reduced to amount of 60%, and therefore sustaining the equal BER performance mainly because in the standard operation condition. Hence, working in the reduced power conditions for less data-rate uses lower than 8 Mbps can result in important energy preserving without the disadvantage of performance degradation.

Table 3 Digital transmission schemes of BCC

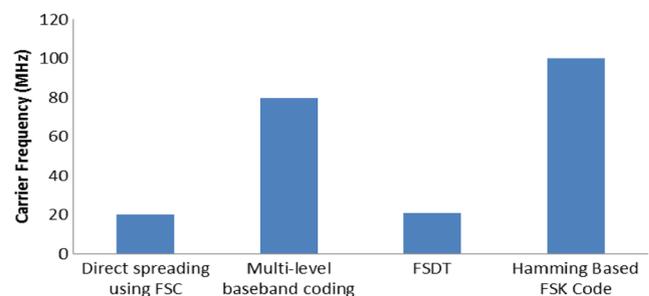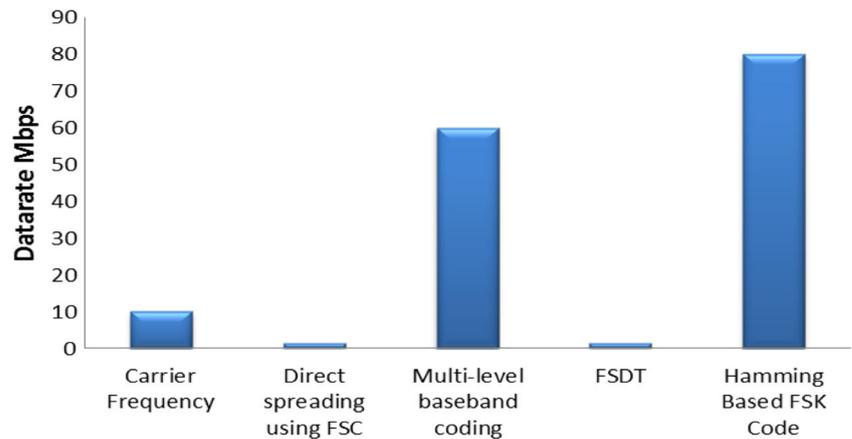| Author	Transmission Methodology	Data rate (Mbps)	Carrier Frequency (MHz)
[19]	Direct-spreading using FSC	1.4	20
[17]	Multilevel baseband coding	60	80
[3]	FSDT	1.4	21
Proposed	Hamming Based FSK Code	80	100

Fig. 14 Variation of carrier frequency in MHz with different techniques

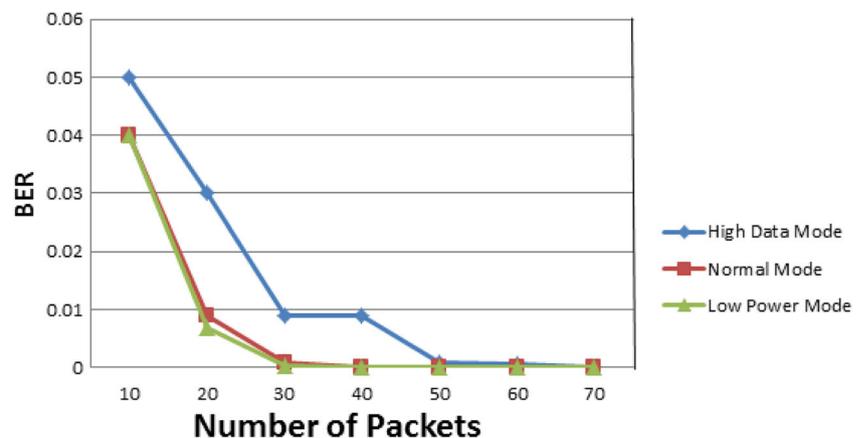**Fig. 15** Variation of data rate in Mbps with different techniques

The HEDT transmitter is designed in an efficient 65-nm CMOS method and it consumes a primary core area of 0.14×0.3 mm. Once operating in the higher data-rate condition, the transmitter utilizes 1.65 mW and the operating power utilization is maintained to at least 1.00 mW in the reduced power condition.

Transmitter power usage savings of 32% is obviously recognized for the reduced power condition compared to the approximated power usage benefits of 41%, which is actually because of employing the power reduction of the digital hamming code block having drastically significantly less than 60% when the clock frequency is decreased by 50%.

For the standard conditions, BER of 10^{-5} is accomplished using the transmitter suggested. For higher data conditions, BER of 10^{-3} is achieved. The HEDT transmitter's efficiency is compared with the latest conventional transmitters which are shown in Table 4 above. The HEDT maintains energy efficiency of 1.00 mW at 60Mbps data rate in 80 MHz Frequency. The proposed highly adaptable Hamming FSK algorithm achieves six occasions of high speed data rate in comparison to other conventional BCC systems.

Conclusion

The Body Channel Communication (BCC) utilizes the human body as a good transmitting medium without the need of additional antennas and complex wiring. It is necessary to achieve a secure and steady communication without depending on channel variants due to various body postures and conditions. In this paper, a flexible power efficient HEDT for BCC is proposed. The HEDT provides high-proficiency data rate of 10 Mb/s at reduced power of 1.00 mW. The data rate shall be increased up to 80 Mb/s under good channel circumstances, using hamming encoding algorithm. The feature of code stacking and harvesting energy from harmonic frequencies are used to increase higher data rate and to decrease power. In this paper, addition to these features hamming codes is placed on direct base band method which is proposed and implemented.

In future strength harvestings featured physique channel communication ought to be implemented to avoid and reduce the overall leakage power. High-speed data rate could be achieved utilizing the Internet of Things (IoT) enabled connection transceiver in BCC systems.

Fig. 16 Comparison of bit error rate performance for three operation conditions

Table 4 Performance summary

Parameters	[22]	[4]	[11]	This Work
CMOS nm	180	130	180	65
Supply Voltage	1 V	1.2 V	1 V	1.1 V
Modulation Scheme	AFH FSK	Frequency Correlation	Double FSK	Hamming FSK
Frequency	30-120 MHz	1-30Mhz	4-120 MHz	4-80 MHz
SIR	-65 dB	-60 dB	-62 dB	-56 dB
Data Rate	10Mbps	8.5Mbps	10Mbps	60Mbps
Power usage	2.4 mW	0.6 mW	2 mW	1.00 mW

Compliance with Ethical Standards

Conflict of Interest   Author 1 declares that she has no conflict of interest. Author 2 declares that he has no conflict of interest.

Ethical Approval   This article does not contain any studies with human participants or animals performed by any of the authors.

Publisher's Note   Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

References

1. Abolhasan, M., Lipman, J., Smith, D., and Jamalipour, A., Wireless body area networks: A survey. *IEEE Commun. Surv. Tutor.*, 16 (3), Third quarter, 2014.
2. Seyedi, M., Kibret, B., Lai, D. T. H., and Faulkner, M., A survey on intrabody communications for body area network applications. *IEEE Trans. Biomed. Eng.* 60(8):2067–2079, 2013.
3. Viittala, H., Hämäläinen, M., and Iinatti J., Impact of difference in WBAN channel models on UWB system performance. *Int. Sym. Spread Spectrum Tech. Applic.*, 1015–1030, 2010.
4. Saadeh, W., and Altaf MAB., A 1.1-mW ground effect-resilient body-coupled communication transceiver with Pseudo OFDM for head and body area network. *IEEE J. Solid-State Circ.* 2690–2702, 2017.
5. Zimmerman, T. G., Personal area networks: Near-field intrabody communication. *IBM Syst. J.* 35(3–4):609–617, 1996.
6. Zimmerman, T. G., Applying electric field sensing to human–computerinterfaces. *Proc. CHI*, pp. 280–287, 1995.
7. Musavi, F., and Eberle, W., Overview of wireless power transfer technologies for electric vehicle battery charging. *IET Power Elect.* 7(1):60–66, 2014.
8. Xie, L., Shi, Y., Hou, Y. T., and Lou, A., Wireless power transfer and applications to sensor networks. *IEEE Wireless Commun.* 20(4):140–145, 2013.
9. Wang, J. et al., Analysis of on-body transmission mechanism and characteristic based on an electromagnetic field approach. *IEEE Trans. Microwave Theor. Tech.* 57(10):2464–2470, 2009.
10. Shinagawa, M. et al., A near-field-sensing transceiver for intrabody communication based on the electrooptic effect. *IEEE Trans. Instrum. Meas.* 53(12):1533–1538, 2004.
11. Maity S., Chatterjee B., and Chang, G., A 6.3pJ/b 30Mbps −30dB SIR-tolerant broadband interference-robust human body communication transceiver using time domain signal-interference separation. *IEEE Custom Integ Circ. Conf.* 230–242, 2018.
12. Baldus, H., et al., Human-centric connectivity enabled by body-coupled communications. *IEEE Commun. Mag,* 172–178, 2009.
13. Bae, J., and Yoo, H. J., The effects of electrode configuration on body channel communication based on analysis of vertical and horizontal electric dipoles. *IEEE Trans. Microwave Theor. Tech.* 63(4):1409–1420, 2015.
14. Timmermann, J., Pancera, E., Adamiuk, G., Wiesbeck, W., and Zwick, T., Estimated performance of UWB impulse radio transmission including dirty RF effects. Proc. *IEEE Conf. Ultra-wideband (ICUWB).* 205–208, 2008.
15. Zhang, L., Liu, X., Huang, J., and Wang, L., Baseband system for human body channel communication. *Proc. Biomed. Eng. Inform. (BMEI)*, 778–781, 2010.
16. Tsai P-Y., Chang, Y-Y., Hsu, S-Y., and Lee, C-Y., An OFDM-based 29.1Mbps 0.22nJ/bit body channel communication baseband transceiver. *VLSI Design, Auto., and Test (VLSI-DAT)*, 815–821, 2015.
17. Shikada, K., Jianqing, W () Development of human body communication transceiver based on impulse radio scheme. Proc. *2nd IEEE CPMT Symp.,* Japan. 1–4, 2012.
18. Tsou, Y. L., Siyong, C., Gong, A., Cheng, N. C., and Lee, Y., Integrated biosensing platform based on a 1.74-mW −90-dBm sensitivity dual- mode-operation receiver for IEEE 802.15.6 Human Body Communication Standard. *IEEE Sensors J* 15(6):3317–3327, 2015.
19. Hyoung, C. H., Kang, S. W., Park, S. O., and Kim, Y. T., Transceiver for human body communication using frequency selective digital transmission. *ETRI J.* 34(2):216–225, 2012.
20. Anzai, D., Katsu, K., Chavez-Santiago, R., Wang, Q., Plettemeier, D., Wang, J. et al., Experimental evaluation of implant UWB-IR transmission with living animal for body area networks. *IEEE Trans. Microwave Theor. Tech.* 61(1):183–192, 2013.
21. Tengfei, L., Zedong, N., Wenchen, W., Feng, G., and Lei, W., A human body communication transceiver based on onoff keying modulation. *Proc. Int. Symp. Bioelectron. Bioinform. (ISBB)*. 61–64, 2011.
22. Namjun, C., Jeabin, L., and Yan, L., A 60kb/s-to-10Mb/s 0.37nJ/b adaptive-frequency-hopping transceiver for body-area network. IEEE Int. Solid-State Circ. Conf. - Digest Tech. Papers, 801–816, 2008.