ASIC modelling of SENSE for parallel MRI

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ABSTRACT

Magnetic Resonance Imaging (MRI) is widely used in medical diagnostics and image reconstruction is a vital part of MRI systems. In Parallel MRI (pMRI), imaging process is accelerated by acquiring less data (undersampled) using multiple receiver coils and offline reconstruction algorithms are applied to reconstruct the fully sampled image. In this research, an Application Specific Integrated Circuits (ASIC) model of SENSE (a pMRI algorithm) is presented which reconstructs the image from the undersampled data right on the data acquisition module of the scanner. The proposed ASIC HDL architecture is compared with SENSE reconstruction model implemented on FPGAs, Multi-core CPU and Graphics Processing Units. The proposed architecture is validated using simulated brain data with 8-channel receiver coils and a human cardiac dataset with 20-channel receiver coils. The quality of the reconstructed images is analyzed using Artifact Power (0.0098), Peak Signal-to-Noise Ratio (53.4) and Structured Similarity Index (0.871) which validate the quality of the reconstructed images using the proposed design. The results show that the proposed ASIC HDL SENSE reconstruction model is ~8000 times faster as compared to the multi-core CPU reconstruction, ~700 times faster than the GPU implementation and ~16 times faster as compared to the FPGA reconstruction model. The proposed architecture is suitable for image reconstruction right on the data acquisition system of the scanner and will open new ways for faster image reconstruction on portable MRI scanners.

1. Introduction

Conventionally, Magnetic Resonance Imaging (MRI) requires significantly a large amount of time for data acquisition. Decreasing the data acquisition time is vital to increase patient comfort. Parallel MRI (pMRI) is a widely used technique to accelerate the data acquisition process, while maintaining the image quality [1]. In pMRI, the acquisition time is reduced by using under-sampling at the cost of additional reconstruction computation. Over the past few years, a lot of research has been done in the field of pMRI and different methods (GRAPPA, SMASH, PILS etc) have been proposed to reconstruct MR images from the under-sampled data [2–6]. SENSitivity Encoding (SENSE) is a standout method which is clinically used to accelerate the MR imaging process.

Normally, the efficiency of an MRI system is determined by the speed at which the data is acquired, and the time taken by the system to reconstruct the fully sampled images. Fast data acquisition techniques (like pMRI) result in aliasing artifacts; therefore different reconstruction algorithms are used to get the fully sampled images. SENSE is a computationally intensive algorithm because it sequentially estimates all the pixel values of the resulting image from the acquired under-sampled

data [1]. It is of course desirable to have an advanced reconstruction platform that would be capable of handling computationally complex reconstruction algorithms in a reasonable amount of time. In recent literature, the use of multi-core Central Processing Units (CPUs), Graphics Processing Units (GPUs) and Field Programmable Gate Arrays (FPGAs) has been proposed to increase the reconstruction speed and to provide real-time image reconstructions [1,6–10].

In current MRI systems, the signals are received by the receiver coils, they are sampled at a certain frequency and then transmitted to a processing module for further processing. These processing platforms are normally CPUs or GPUs where the off-line reconstructions are performed [9,10]. Limin Li et al. proposed to use FPGAs for real-time image processing [11]. Siddiqui MF et al. Proposed to use FPGAs for SENSE algorithm [7,8]. Dalal et al. Proposed a 16-channel front end for MRI scanners [12]. The proposed front end in [12] can be modified to incorporate reconstruction architectures.

Researchers around the globe are using different tools to automate digital systems. Automating the physical layout of a digital design is an important task when weeks may be required to design a single chip, which reduces the burden of design engineers [13]. The design size for System-on-Chip (SoC) has increased significantly over the years (almost
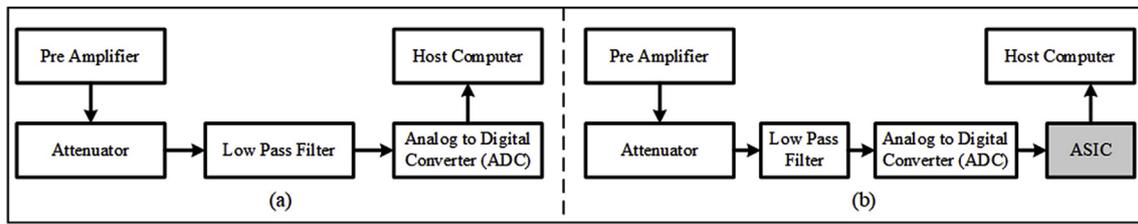
Fig. 1. MRI front end hardware (a) conventional approach where the undersampled data is transferred to the host computer for processing (b) the proposed approach, where image reconstruction is performed in the signal processing chain of the MRI scanner. Only the reconstructed images are transferred to the host computer for storage and printing.

58% in a period of 6 years), while the Application Specific Integrated Circuit (ASIC) design tools have increased the productivity of an individual engineer (defined by the number of transistors designed in a month) only by 21%. So, to overcome this productivity gap and to design ASIC for complex algorithms (e.g. SENSE), a recent trend is to rely more on automatic tools (e.g. SoC Encounter from Cadence Inc) to generate the physical layout for ASIC [14].

MRI systems can benefit from efficient hardware platforms for real-time processing as proposed in [7,8,11]. The acquired undersampled data can be reconstructed within the signal processing chain of MRI data acquisition process as shown in Fig. 1. In a conventional process of MRI data acquisition (Fig. 1a), the received signals after initial processing (amplifying, attenuating and filtering out the unwanted signals [15]), are sent to a host computer for image reconstruction. Conventionally, the data is transmitted to a processor using either fiber optical cable or using coaxial cables [16–19]. In fiber optics setup, the data is taken out from the exam room using a waveguide, which degrades the signal quality [18]. While the transmission system based on coaxial cables is complex. More cables are required if the number of receiver coils is increased [19]. The coaxial cable network has to be routed in a room dynamically, adding noise in the signal due to bending [19]. This paper provides a design to perform image reconstruction right on the receiver coil data acquisition system by the addition of a chip (ASIC) as shown in Fig. 1b.

Normally, FPGA devices have a limited number of generic logic cells and the input/output blocks which restricts the use of FPGAs for computationally intense image processing algorithms [20]. ASICs provide an alternative to the FPGAs for real time processing. ASIC designs are normally targeted to achieve better quality results using less computation time and consuming less power.

In this paper, an ASIC architecture is proposed for SENSE algorithm to be used for reconstructing the fully sampled images from the acquired pMRI undersampled data right on the receiver coil system of an MRI scanner. The proposed ASIC architecture is designed to perform real-time processing with the existing front-end hardware of an MRI scanner. The proposed architecture can be used for applications where images are required without any time delay such as in portable MRI scanners where images are swiftly acquired, and real-time reconstruction is desired to generate MR images immediately on run-time.

2. Theory

SENSitivity Encoding (SENSE) is one of the algorithms used in parallel MRI which reconstructs images from the undersampled pMRI data acquired using multiple receiver coils [21,22]. SENSE is an image domain reconstruction method, where multi coil aliased images are obtained by applying inverse Fourier Transform (iFFT) on the acquired undersampled *k*-space data. The receiver coil sensitivity profiles are used to approximate the aliased signal components in the folded images. The estimated pixel values are allocated to the right pixel locations to get the fully sampled image as shown in Fig. 2 (which depicts the case for 2 receiver coils and acceleration factor 2). Equations (1) and (2) can be used to formulate a solution to estimate the missing
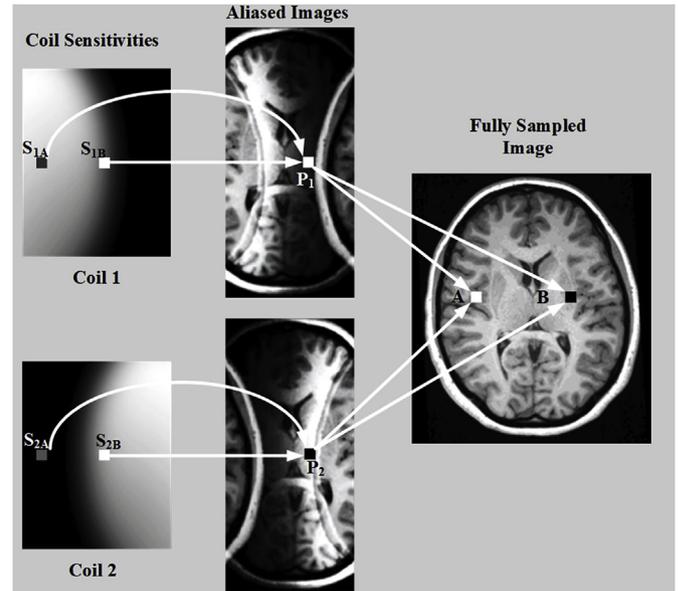

Fig. 2. SENSE reconstruction process to estimate the missing pixel values (A and B) of the reconstructed image using receiver coil sensitivities (S_{1A}, S_{1B}, S_{2A}, S_{2B}) and aliased images (P_1 and P_2) obtained from the undersampled data.

points (shown in Fig. 2) in the full FOV image.

$$P_1 = A. S_{1A} + B. S_{1B} \tag{1}$$

$$P_2 = A. S_{2A} + B. S_{2B} \tag{2}$$

In equations (1) and (2), P_1 and P_2 represent the undersampled MRI data acquired from the MRI scanner, S_{1A}, S_{1B}, S_{2A} and S_{2B} are the corresponding weights obtained from the receiver coil sensitivity profiles. These equations can be written in a matrix form as:

$$\begin{bmatrix} P_1 \\ P_2 \end{bmatrix} = \begin{bmatrix} S_{1A} & S_{1B} \\ S_{2A} & S_{2B} \end{bmatrix} . \begin{bmatrix} A \\ B \end{bmatrix} \tag{3}$$

Equation (3) can be written as: $P = S. A$, where P is the acquired data from the scanner, S matrix is the sensitivity encoding matrix and M is the solution image. The solution to equation (3) can be given as:

$$A = S^{-1}. P \tag{4}$$

In equation (4), the dimensions of S depend on the number of receiver coils (number of rows) and the acceleration factor (number of columns). In Cartesian trajectories, the number of receiver coils need to be always more than the acceleration factor [23], therefore forming an inverse encoding matrix S is required to find the solution image.

2.1. Image reconstruction platforms for MRI scanners

In conventional MRI systems, CPUs are being used to reconstruct images from the acquired data as part of the MRI scanner. CPU is a

general-purpose processing element, therefore, the processing of data on CPU is slow as it processes different operations MR image reconstruction. GPUs provide an alternate and fast simulation platform to speed up the image reconstruction process. The CPUs and GPUs have a limitation that they cannot be embedded within the data acquisition system of MRI scanner, therefore, in both these technologies all the raw data must be transferred from the data acquisition system to the workstation for reconstruction.

FPGAs provide a platform to design and test prototypes for different applications and can be used for MR image reconstruction. They can be embedded on the receiver coil data acquisition system of the MRI machines, which allows to start reconstruction process right on the receiver coil data acquisition system and there is a no need to transfer all the raw data. Application Specific Integrated Circuit (ASIC) is a custom-made chip designed for a specific purpose, consumes low power (9–12 times less than FPGAs), requires less area (21–40 times lesser than FPGA design) and provides faster computation times (2.1–4.5 times faster than FPGA) [19]. The target specific application of ASIC has a smaller form factor as the device is manufactured for a specific algorithm. ASIC supports both the analog and digital designs which is not possible in FPGAs where the type of architecture (analog or digital) is fixed by the vendor. ASICs are more suitable for the projects having complex architectures (e.g. SENSE algorithm) than FPGAs because FPGAs have limited resources [24].

3. Methods

ASICs provide a high speed and low power architecture to process complex problems e.g. advance MRI algorithms. A low power and compact ASIC is suitable for MRI scanners to reconstruct the data in real-time with better SNR and reduced operational costs.

3.1. Proposed architecture of SENSE algorithm

SENSE reconstruction algorithm can be implemented using two major blocks as proposed in [25]: (i) pseudo inverse module (to compute the inverse of the encoding matrix) and (ii) multiplier module (for the multiplication of the inverted encoding matrix with the undersampled data). On-chip memories can be used to fastly access the data (sensitivity encoding matrix of receiver coils and undersampled data from the scanner), and to process the data more effectively as compared to conventional systems.

The proposed architecture of SENSE consists of four different modules (memories, pseudo inversion, multiplication and control circuit) as shown in Fig. 3. The architecture uses three memories which store input data and the resultant image. Pseudo inversion module computes the inverse of the encoding matrix which is then multiplied with the undersampled data using the multiplier module. 'Control Circuit' module is used to control the overall memory access and the processing of all the other modules.

'Memory 1' is a dual port read and write access two-dimensional random-access memory (2D-RAM), which is used to store the encoding matrix. Undersampled data is stored in a dual port read and write access 2D-RAM (Memory 2) as shown in Fig. 3. Read and write access to the memory is controlled through 'Control Circuit' module. The module performing the inversion of the encoding matrix (S) and its multiplication with the undersampled data (P) is shown in Fig. 4, where the pseudo inverse module shows block diagram of the left pseudo inverse [26] operation used to perform matrix inversion. The left pseudo inverse method includes taking the transpose of a complex matrix (encoding matrix). The pseudo inverse module includes multiplication of the complex matrices (S^T and S) which provides a square matrix and a module to invert the square matrix. In Fig. 4, the encoding matrix S is obtained by taking two weights (for acceleration factor 2) from the sensitivity maps (stored in memory 1) of each receiver coil (8 receiver coils) which results in a rectangular encoding matrix of size 8×2.

The *Transpose* module performs the complex conjugate transpose of S by rearranging the points within the matrix and provides a complex transposed matrix S^T. The transposed rectangular matrix S^T is multiplied with S to get a square matrix of dimension 2×2. For performing the complex multiplication in this paper, the architecture proposed by Siddiqui et al. is used [7].

The inversion of the square (2×2 for $A_f = 2$) matrix is achieved using the simplest matrix inversion method (pseudo left inverse [27]), where the determinant of the matrix is multiplied with its adjoint [25].

Similarly, the acquired undersampled data (P) is obtained by taking one aliased pixel from the undersampled image of each receiver coil which then results in an 8×1 vector (for 8 channel receiver coils). A complex matrix multiplier is used to multiply the sensitivity encoding matrix (S^{-1}) with the corresponding undersampled data vector P (memory 2), to get the solution pixels (2 points for $A_f = 2$) in image A (Memory 3). Once the relevant pixel values of the solution image are obtained, the resultant image is stored in Memory 3 (shown in Fig. 7). Memory 3 is also similar (2D-RAM) to the other two memories (Memory 1 and 2). Read and write access to the memory is controlled using '*sense_done*' signal through 'Control Circuit' module.

3.1.1. Control circuit

Control Circuit mainly consists of control signals used to control the read and write access to the memories, pseudo inversion and multiplication modules and to read data at the output. The control circuit is designed using two interconnected Finite State Machines (FSMs).

Finite State Machine to read Sensitivity Encoding Matrix:

The Finite State Machine (FSM) shown in Fig. 5 is used to read the receiver coil sensitivity encoding matrix in Memory1. The FSM is a four-state (S0, S1, S2 and S3) machine which generates different control signals to manage access to Memory 1. The description of each state is given below:

- State 0 (S0)

This state is used to erase all the garbage values from the required register memories. The *reset* signal is active high, which holds the state until the signal is low. The state is also on hold until the sensitivity encoding matrix is available at the input ports, which is indicated with a high signal at *f_data* port. Once the sensitivity encoding matrix is available, the state is updated, and the system shifts to State 1.

- State 1 (S1)

In State 1, *f_start* and *count_ud* are updated. *f_start* signal activates Memory1 to read the sensitivity encoding matrix while the *count_ud* is used to control the number of data bits to be read in the next state, so the counter is initialized by zero.

- State 2 (S2)

The machine remains in State 2 until the sensitivity encoding matrix has been read in Memory 1. Here *count_ud* is used to control the state of the machine which must be in S2 until *count_ud* value is less than $(A_f \times width + 2) \times ny$. Here, *width* is the word length used to represent one number, *ny* defines the number of points to be recovered in one iteration and A_f is the acceleration factor of the undersampled data.

- State 3 (S3)

In this state, a flag (*fdata_ready*) is triggered and a high flag is sent to the second FSM, which controls the reading of the undersampled data and execution of the SENSE algorithm.

Finite State Machine to read Undersampled Data and to compute SENSE algorithm.

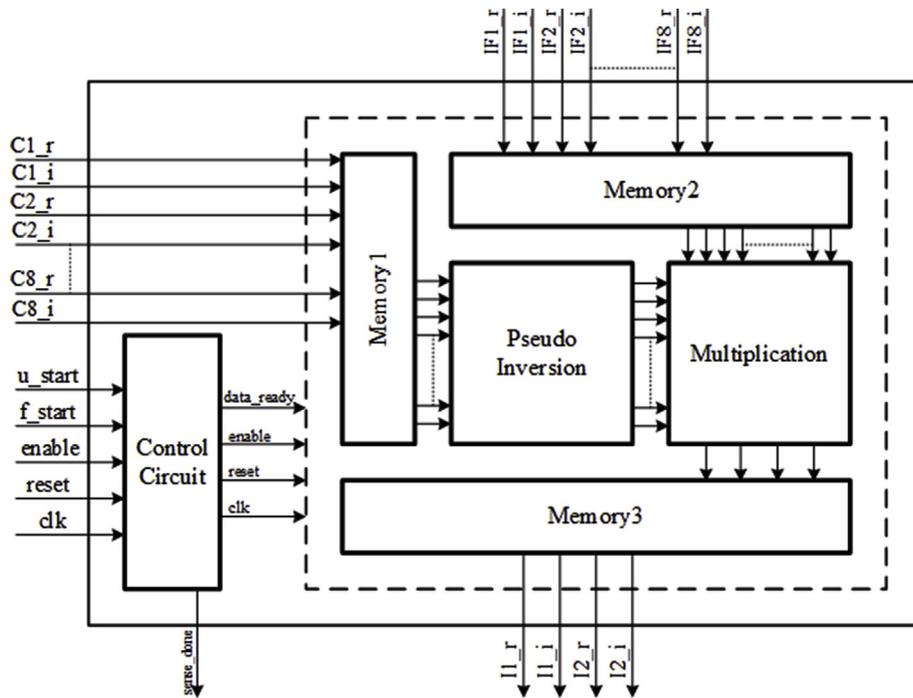The FSM used to read the undersampled data is shown in Fig. 6. The

Fig. 3. The proposed architecture of SENSE algorithm.

FSM reads data in Memory 2 for multiplication with the inverse of the encoding matrix. This FSM has six-states (S0, S1, S2, S3, S4 and S5) which generate different control signals to manage access to Memory 2. This FSM controls the reading of the undersampled data in Memory 2 and enables the execution of SENSE reconstruction algorithm when the data (encoding matrix and undersampled data) is available in memories. This FSM also controls the writing of the resultant image to Memory 3. The description of each state is given below:

- State 0 (S0)

All the garbage values in registers are cleared at this state. The *reset* signal is active high. The state does not change until the undersampled data is available at the input ports. The availability of the undersampled data is indicated by a flag signal *'c_data'*. When the undersampled data becomes available at the input ports, the state is updated, and the system shifts to State 1.

- State 1 (S1)

In this state, *u_start* and *count_cd* are updated to read the undersampled data. The *u_start* (connected to rd/wr port of Memory 2) signal activates Memory 2 to read the undersampled data. The *count_cd* is initialized by zero as this will be used to control the number of the bits for each pixel.

- State 2 (S2)

The FSM remains in State 2 until the undersampled data has been read fully in Memory 2. Here *count_cd* controls the state of the machine. The machine must stay in S2 until *count_cd* value is less than: $A_f \times width \times ny$. Here *width* is the word length used to represent one number, *ny* defines the number of points to be recovered in one iteration and A_f is the acceleration factor of the undersampled data.
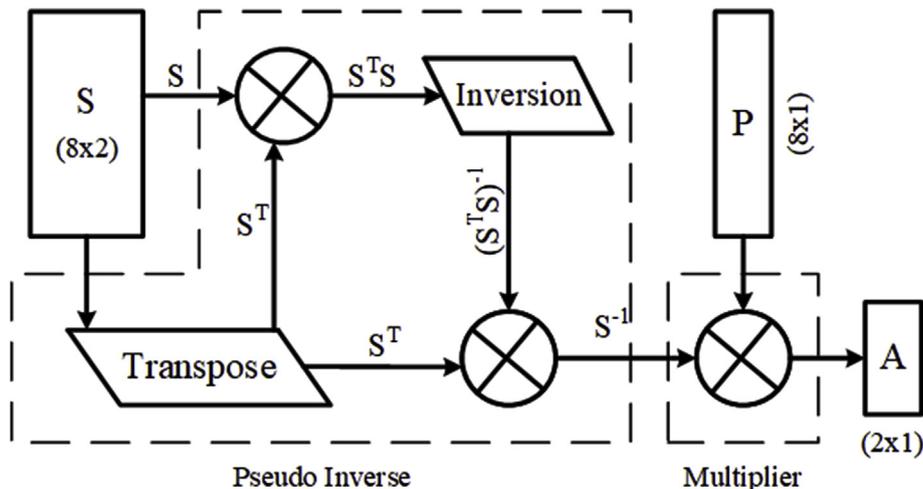

Fig. 4. Reconstruction process for 8 receiver coil data with acceleration factor 2. Pseudo Inverse is used to invert the encoding matrix (S). The resultant image (A) is obtained by the multiplication of S^{-1} with the undersampled data P.
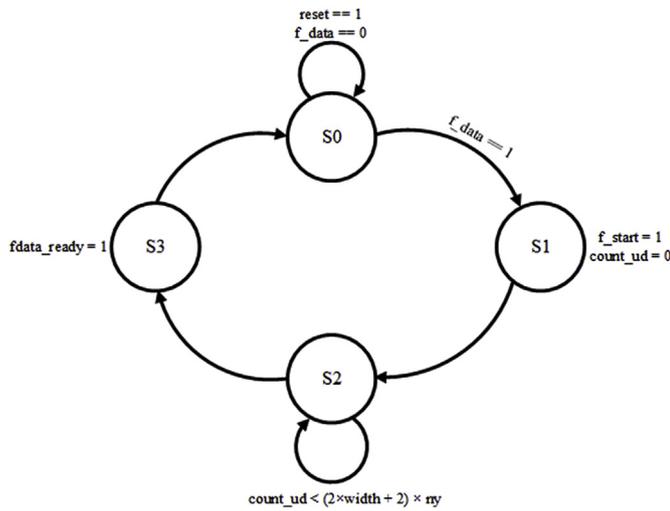
Fig. 5. Finite State Machine (FSM) used to read sensitivity encoding matrix in Memory 1.
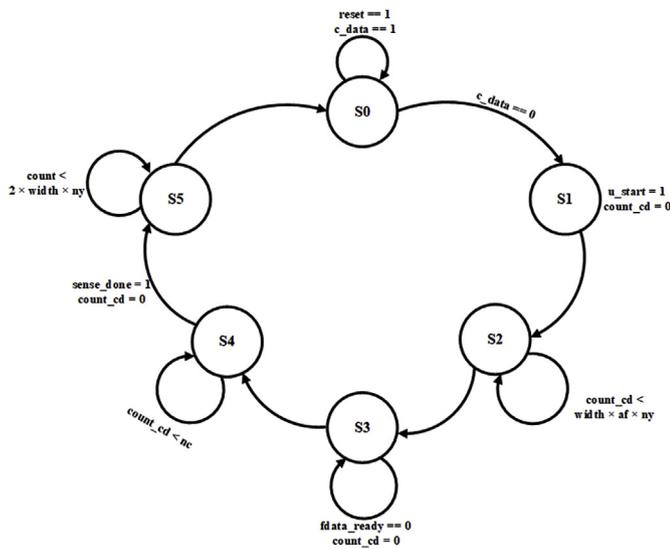

Fig. 6. Finite State Machine (FSM) to read the undersampled data in Memory 2 and to control the execution of SENSE algorithm.

- State 3 (S3)

In State 3, the system waits for the sensitivity encoding matrix to be ready in Memory 1. The flag *fdata_ready* from the first FSM will indicate once the sensitivity encoding matrix is available for further processing. When *fdata_ready* signal is high, the counter is reset to zero and the state is changed to State 4.

- State 4 (S4)

State 4 runs for *nc* clock cycles, which is the number of receiver coils. The modules (pseudo inverse and multiplication) used for SENSE algorithm are not dependent on the clock signal, the system waits for a few clock cycles to make sure that SENSE reconstruction is executed properly. After *nc* clock cycles, a flag '*sense_done*' is updated to indicate the successful execution of SENSE algorithm and the state is updated to State 5.

- State 5 (S5)

The final state of the FSM is to write the resultant image after SENSE reconstruction in Memory 3. The FSM remains in State 5, until the complete image data is written in Memory 3. The resultant data has A_f pixels, each of which has a size of '*width*'. In S5 of FSM, n_y defines the number of pixels to be reconstructed at a time.

3.2. ASIC design of SENSE architecture

In this paper, an ASIC implementation of SENSE algorithm for 8 receiver coils with acceleration factor 2 is presented. The proposed architecture is designed with RTL language (Verilog). Verilog netlist of the proposed architecture is generated using Design Vision, a tool from *Synopsys ®*, and SoC Encounter from *Cadence Inc* is used to generate the ASIC layout from Verilog netlist. The overall design flow of the Cadence Encounter for SENSE reconstruction is shown in Fig. 7.

3.2.1. Technology for the proposed ASIC layout

It is important to decide which technology to be used during the layout process of the proposed SENSE architecture. The proposed design uses 65 nm process for ASIC designing so that the SENSE architecture could be used with the existing front-end designs of MRI scanners. The operating parameters used for the proposed SENSE architecture are given in Table 1.

3.2.2. Key parameters for ASIC layout

SoC Encounter uses different input parameters to successfully design the ASIC layout. It requires a Netlist file generated from Design Vision which contains the definitions of physical cells at gate level. The design vision also tells the SoC Encounter about the delays and rise and fall time of the design. All the chip parameters used to design the ASIC layout are given in Table 2.

3.3. Experimental setup

ModelSim is used to test and verify the proposed ASIC architecture for SENSE algorithm. The simulation platform shown in Fig. 8 is used to test the performance of the proposed HDL architecture. The simulated brain and cardiac perfusion dataset (converted to ModelSim readable files by using file writer model) are fed to the proposed SENSE
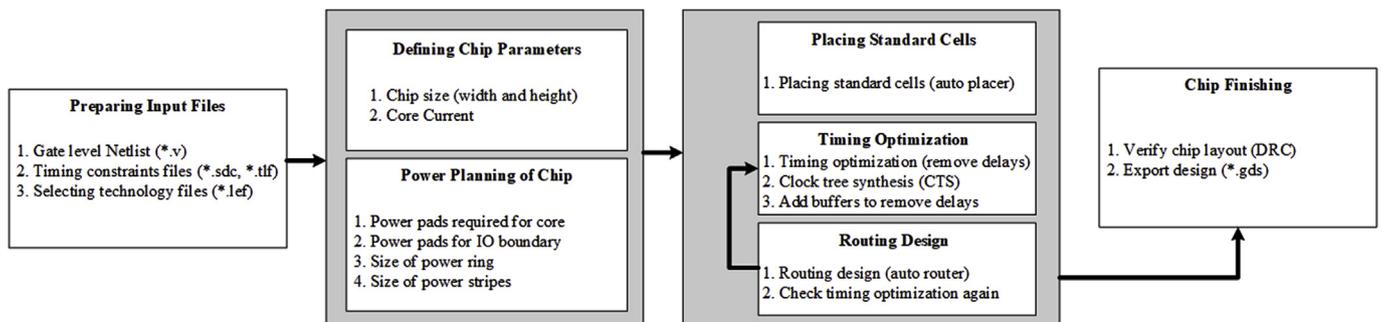

Fig. 7. Automatic design Flow of Cadence's SoC Encounter (from input files to chip finishing) for the proposed architecture.

Table 1
Operating conditions for the proposed ASIC architecture of SENSE.

Technology	Frequency MHz	Minimum Operating Voltage	Maximum Operating Voltage	Minimum Temperature (C)	Maximum Temperature (C)
65 nm	100	0.90 V	1.02 V	−40C	105

architecture. The reconstruction results computed by the proposed design are stored in the text files for validation purposes. The resultant images are then transferred to the system for quality validation and to display it on the screen.

4. Results

The proposed design is tested for cardiac cine dataset, acquired with a 3 TTesla Skyra Siemens scanner at Case Western Reserve University, USA. The dimensions of the dataset are 256×256 and the data was acquired using 30 channel receiver coils. The other dataset used in this paper, to verify the proposed ASIC design, is the simulated human brain dataset with 8 receiver coils (256×256 dimensions). Both the datasets were retrospectively undersampled with an acceleration factor 2. The simulations for ASIC architecture are performed using ModelSim SE 6.5 and the CPU simulations are done using OpenMP and GPU simulations are performed on NVIDIA's TESLA K40c GPU [28]. The processing of both the architectures is performed using Core-i7 CPU (6 GB RAM and 2.7 GHz processor). The results of FPGA are taken from [7].

Fig. 9 shows the reconstruction results of the cardiac and brain datasets using the proposed HDL architecture of SENSE reconstruction. Fig. 9a shows the original cardiac perfusion image and the simulated brain dataset (reference images). Fig. 9b and c shows the reconstruction results for A_f = 2 using CPU and the proposed ASIC model, respectively. The results (artifact power) show that there are no significant differences between the original images and the reconstructed images.

The artifact power, peak signal-to-noise ratio (PSNR) and structured similarity index (SSIM) of the proposed method for both the datasets, shown in Table 3, are in acceptable range. The proposed method provides good quality of the reconstructed images (as shown in Fig. 9) for clinical purposes. The proposed architecture uses 16-bit fixed point decimal representation for pixel representation. The artifact power can further be reduced by using a larger word length with increased fractional bits but at the cost of more processing elements (depends on the actual requirements). By using the optimized word lengths, the processing time can be decreased further.

4.1. Synthesis results

The physical design of the ASIC is implemented using the SOC Encounter tool and 65 nm technology is used for the layout of the proposed design. The overall architecture consists of two main modules i.e. pseudo inverse and multiplication. The layout (including IO pads, power pads, corner pads, power routing wires) of the multiplication, pseudo inversion and overall SENSE algorithm architecture chip is shown in Fig. 10.

In this first generation of ASIC design, we have incorporated the modules which can reconstruct two pixels at one time (typical the case when A_f = 2). The architecture presented in this paper is parameterized to accommodate the reconstruction of multiple pixels at a time with different acceleration factors.

The area, timing and power analysis of the ASIC design are obtained from the Design Vision tool (from Synopsys) and the results (area, gate count and power) are shown in Table 4. All the synthesis is performed using specific libraries for a 65 nm process, as provided by ASIC manufacturers (STMicroelectronics Inc). The total power consumption is the combination of the dynamic power and the leakage power, shown in Table 4.

4.2. Layout of the proposed ASIC architecture

The proposed architecture of SENSE algorithm is compiled using multi-core processor (Intel (R) Zeon (R) 16 Core) and it took 31 h to compile the pseudo-inversion module (Fig. 10b) and approximately 8 h to compile the multiplication module (Fig. 10a). The complete architecture, shown in Fig. 10c, takes 87 h to compile and occupies a core area of approximately 7.43 mm^2.

5. Discussion

In this paper, ASIC implementation of SENSE algorithm is presented. The computation time for the reconstruction of both the datasets taken by the proposed architecture (shown in Table 3) is significantly lesser (only 0.01 ms for brain dataset with 8 channel receiver coil and acceleration factor of 2, and 0.04 ms for cardiac dataset with 30 channel receiver coil and acceleration factor is 2) than the CPU (using multi-core) model of the SENSE reconstruction which took 80 ms and 1420 ms for the same datasets, respectively [28]. The processing power of CPUs (quad core, Core-i7, 2.7 GHz Processor) is limited by the overall processor speed and the sequential nature of processing, as compared to ASIC architectures which are dedicatedly hardware-based and accommodate independent processes efficiently. The proposed architecture also performs better than the GPU reconstruction time claimed in [28]. The proposed model performs 700 times better in terms of reconstruction time when comparing with method proposed in [28]. The proposed architecture also outperforms FPGA in terms of processing time as it takes only 0.01 ms to reconstruct an 8-channel dataset while FPGA takes 0.164 ms for the said task. The proposed model will be easier to embed to the MRI scanners than FPGAs.

Experiments in this research show that the proposed ASIC architecture can reconstruct images with good artifact power, structured similarity index and peak signal-to-noise ratio, which ensures better quality of the reconstructed images. The proposed ASIC architecture reconstructs images faster than multi-core CPU reconstruction. The proposed architecture also has faster processing speed as compared to the CPU implementation of SENSE algorithm [27].

Conventionally, in MRI scanners the acquired raw data (normally in hundreds of Megabytes) is transferred to CPU workstation for image reconstruction. The loss of signal during transmission may cause a decrease in SNR. In current MRI, normally multi-core CPU or GPU systems are used for image reconstruction. The need to transfer a huge amount of raw data for image reconstruction increases the need of memories to
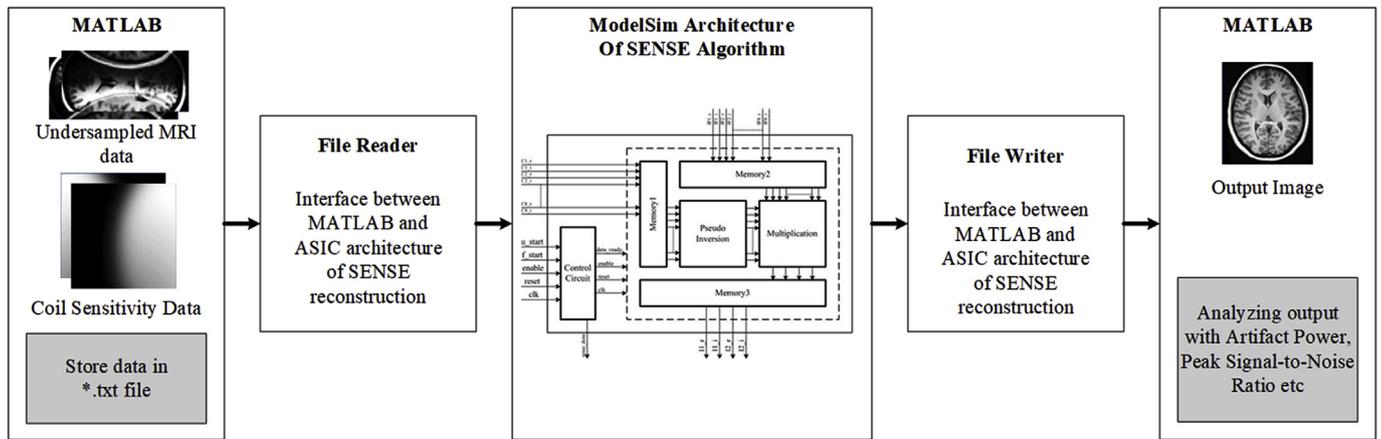
Table 2
Chip parameters used for the proposed SENSE architecture.

Total Power (P_{dyn})	Core Current (I_{core})	Chip Width ($W_b = H_b$)	No. of Power Pads (N_{pd})	Width of Core Ring (W)	Gap Between IO Pads (W_{pt})
mW	mA	um	–	um	um
5.520	5.411	3.26	7	3	3

Fig. 8. Experimental setup used to test and verify the results, where MATLAB is used to generate test matrices and to analyze the reconstructed images. File reader and writer modules are used to send and receive data from SoC Encounter module.
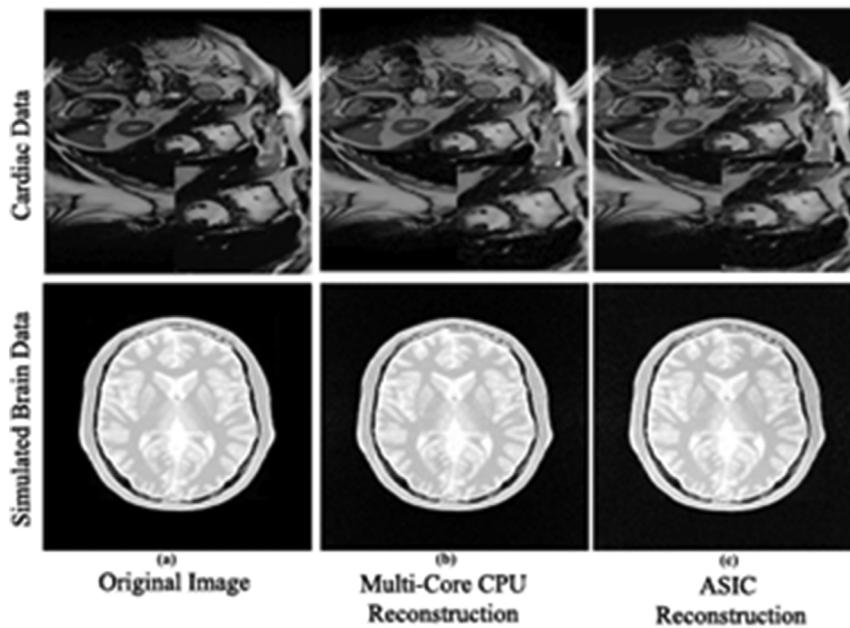

Fig. 9. Reconstruction results of the simulated brain and the 3 T cardiac perfusion dataset with acceleration factor 2: (a) original image, (b) CPU simulations, (c) reconstruction using the proposed ASIC model.

Table 3
Artifact Power (AP), Peak Signal to Noise Ratio (PSNR), Structured Similarity Index (SSIM) and Processing Time comparison using CPU (8 core simulations) [28], Graphics Processing Units (GPUs) [28], FPGA model [7] and the proposed HDL SENSE architecture.

Parameter	Dataset	Simulation Results			
		CPU (8 Core) [28]	GPU Architecture [28]	FPGA Model [7]	ASIC HDL Model
Artifact Power	Simulated Brain	0.0055	0.00002	0.0122	0.0141
	Cardiac Perfusion	0.0031	0.0038	0.0090	0.0098
PSNR	Simulated Brain	49.8	57.6	36.1	49.4
	Cardiac Perfusion	56.1	56.1	53.3	53.4
SSIM	Simulated Brain	0.901	0.926	0.85	0.845
	Cardiac Perfusion	0.894	0.887	0.87	0.871
Processing Time (ms)	Simulated Brain	80	7.46	0.164	0.01
	Cardiac Perfusion	1420	114.55	0.176	0.04

store and process the data. The rate at which the data is transferred using coaxial cables is limited by the length of the cable and the number of channels used for transmission. The cross-talk within the sub channels also reduces the SNR of the transmitted signal.

The advantage of the proposed architecture is the potential to offer real-time MR image reconstruction right on the receiver coil data acquisition system of the MRI scanner. Only the resultant image needs to be transferred to the host machine for printing and storage. It is desirable in MRI scanners to reduce the transmission burden. So, the proposed model will reduce the number of cables required for
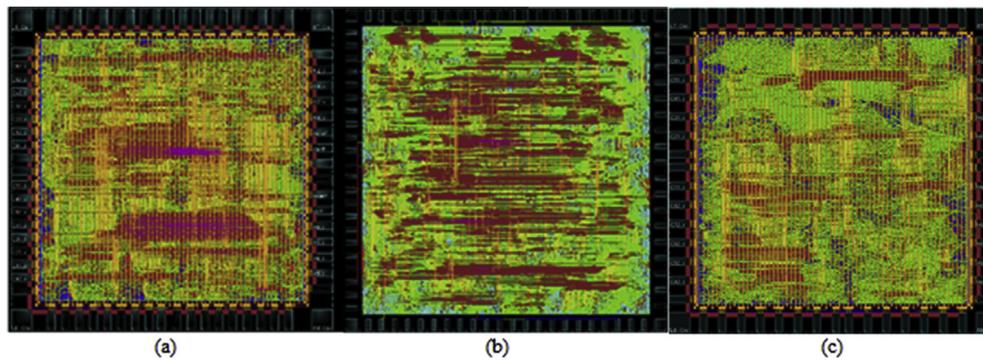
Fig. 10. Physical layout of (a) multiplication module and a (b) pseudo inversion module and (c) SENSE reconstruction architecture.

Table 4

ASIC area (mm^2), Gate Count and Power of Pseudo inversion, multiplier and SENSE architecture.

Module	Total Cell Area (mm^2)	Total Gate Count (Kilo)	Total Power (mW)
Pseudo inverse	5.68	2639	4.816
Multiplier	1.36	632	1.39
SENSE Architecture	7.432	3461	5.520

transmission as only a small amount of data (reconstructed image) will be transferred to the workstation which can be achieved using wireless transmission. The proposed ASIC architecture offers a new approach where the reconstruction is performed in real-time, right within the signal processing hardware and only the reconstructed images are transferred to computers for display.

The proposed architecture can be used with the existing front-end MRI scanner hardware used to process signals for data acquisition. A real-time reconstruction using the proposed architecture is very advantageous for MRI examinations in many ways: (i) this helps the radiologists to detect problems during the MRI scan, thus reducing the operating cost of MRI scanners, (ii) it is also useful for portable MRI scanners which are in development phase where low power, on board ASIC is more valuable, (iii) it will help to increase SNR due to less signal loss.

6. Conclusion

In this paper, a generalized ASIC design for SENSE reconstruction using HDL language is presented. The proposed architecture is capable of reconstructing MR images from the under-sampled data within the signal processing front-end hardware of the MRI scanner, hence reducing the processing time. Experiments show that the proposed design provides comparable image quality with the CPU/GPU reconstruction results. The reduced image reconstruction time (approximately 8000 faster than multi-core CPU simulations, 700 times less than GPU based implementation, and 16 times less than FPGA based solution) enables the use of this design for real-time image reconstruction as well as in portable MRI scanners. The proposed method is also helpful to reduce the SNR in the reconstructed images, because of less MRI raw data transfer for reconstruction. The proposed system has a potential to transmit only the reconstructed images for processing or to printing platforms hence reducing the transmission burden for MRI systems.

Conflict of interest declaration

The authors Dr. Sohaib Ayyaz Qazi, Dr. Muahammad Faisal Siddiqui, Dr. J Jacob Wikner and Dr Hammad Omer have declared that no conflict of interest exist.

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