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Article

A non-volatile AND gate based on $Al_2O_3/HfO_2/Al_2O_3$ charge-trap stack for in-situ storage applications

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ABSTRACT

The emergence of two-dimensional (2D) materials has inspired academia in microelectronics to find a novel device structure to offer a potential technological route for increasing energy efficiency and processing speed for data storage and computing at transistor level. Devices based on 2D materials include logic gates and memories, each with their own unique features. However, integrating logic function and memory into a single device has barely been studied. Here, we report a non-volatile AND gate based on $Al_2O_3/HfO_2/Al_2O_3$ charge-trap stack. The device can store charges after completing logic operation. The ratio of high and low current states during logic operations can exceed 10^5. The output current states during the logic and memory operations still have a two orders of magnitude distinction after 800 s, indicating that this device possesses the non-volatile characteristic. The device has potential applications for in-situ memory applications, which makes it a possible candidate to break the "memory wall" at transistor level.

1. Introduction

Over the past few decades, computing performance has continuously improved based on complementary metal oxide semiconductor (CMOS) transistors, mainly by the continual scaling down of feature size of the transistors, as predicted by Gordon Moore [1]. However, hardware processing and data storage happen in different components (process unit and memory unit) inside the chip; von Neumann architecture has ruled the computing fabric until now. Nowadays, the performance gap between processors and memories is becoming larger and larger, greatly impeding the computing power of microprocessors [2–5]. In von Neumann architecture, the constant data exchange between processing units and memory units limits the speed and the energy efficiency, which is called the "von Neumann bottleneck". In addition, the performance mismatch in different units in von Neumann architecture causes data collapse, which is generally referred to as the "memory wall". Recently, researchers have come up with many different integrated structures to overcome this problem, including logic in memory [6,7], intelligent memory [7,8] and process in memory [9,10]. Although these different architectures are beneficial in addressing memory capacity and memory speed, they also bring new problems, such as the data-access bottleneck.

According to the International Technology Roadmap for Semiconductors (ITRS 2.0), materials with high mobility and controlled interface states will become promising candidates for next generation semiconductors. 2D materials like MoS_2, WSe_2 and BN have unique electrical [11–16] and optoelectronic properties [17–19]. Various electrical devices like flash memory devices [20–24], neuromorphic devices [25–30] and p-n diodes [17,31–34] have been developed. In addition, research on 2D materials in memory devices is not limited to a single transistor. Other research which combines the logic cell and storage performance also shows promising application prospects. In 2015, Lee et al. [35] reported a high performance non-volatile inverter based on electrode-contacted 2D MoS_2 and black phosphorus combined with ferroelectric P(VDF-TrFE). However, for integrating logic and memory in a single device, very little research has been reported. Aiming to break the "memory wall" in von Neumann architecture, new technology based on novel materials has not yet been realized.

In this work, we developed a novel non-volatile AND gate based on $Al_2O_3/HfO_2/Al_2O_3$ charge-trap gate stack. Here, $Al_2O_3/HfO_2/Al_2O_3$ gate stack can trap and release carriers, which will cause the current state to change in the channel. Together with the AND gate logic, in-situ memory [36] is realized. The device not only shows the AND logic characteristic, but also exhibits non-volatile memory performance, indicating that charges can be stored after logic operations. Such a device has potential value for in-situ memory applications.

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2. Experimental

2.1. Preparation of $Al_2O_3/HfO_2/Al_2O_3$ charge-trap stack

The heavily doped Si substrate with ≈300 nm thermally oxidized layer was used for the fabrication of the device to ensure electrical insulation between two buried gates. First, patterns of two separated gates served as logic inputs were fabricated through electron beam lithography (EBL) using polymethyl methacrylate (PMMA) (AR-679.04) polymer. After that, 5 nm Cr and 30 nm Au were deposited on the patterned sample through e-beam evaporation (EBE). Then, the sample was immersed in acetone for lift-off process. After the fabrication of two separate buried metal gates, the first Al_2O_3 layer (the thickness was 12.5 nm) was deposited on the sample via atomic layer deposition (ALD). During the ALD fabricating process, trimethylaluminum (TMA) was reacted with water at 300 °C for the Al_2O_3 layer. Then, the HfO_2 layer (the thickness was 3 nm) was deposited on the Al_2O_3 layer by ALD, during which the tetrakis(ethyl-methylamido) hafnium reacted with water at 250 °C to form HfO_2 film. Finally, the Al_2O_3 layer (the thickness was 7 nm) was deposited on the top of HfO_2 based on the reaction of the TMA and the water at 300 °C.

2.2. Preparation MoS_2 channel material and source/drain electrodes

The channel material MoS_2 was acquired by mechanical exfoliation on a silicon wafer and transferred to the sample with two buried gates and $Al_2O_3/HfO_2/Al_2O_3$ charge-trap stack. During transfer process, the channel MoS_2 should be aligned on the top of two parallel buried gates with the help of a water-soluble layer (PVA). Then, the sample was soaked in the deionized water for 40 min to remove the PVA film. The drain and source electrodes of the device were firstly patterned by EBL and the 5 nm/30 nm Cr and Au were deposited by EBE method. After the lift-off process, the device was fabricated successfully. The detailed fabrication process is shown in the supplementary material (Fig. S1 online).

2.3. Device electrical measurement

The electrical properties of the device were measured in the probe state with the semiconductor parameter analyzer (Keithley 4200A). The voltage pulses were generated by the source-measure units (SMU) of the Keithley 4200A.

3. Results and discussion

Fig. 1a is a schematic of the device structure of the non-volatile AND gate. Two separate buried metal gates control the MoS_2 channel independently. Then the dielectric layer is the stack of $Al_2O_3/HfO_2/Al_2O_3$ (AHA). The thickness of each layer is about 7 nm/3 nm/12.5 nm, respectively. Here, the top layer (7 nm Al_2O_3) serves as the tunneling layer. The HfO_2 layer serves as the charge trap layer. Charges tunneled from the channel can be stored in this layer. Finally, the down most Al_2O_3 layer (12.5 nm) serves as the blocking layer. Two separate buried metal gates, which control the corresponding part of the MoS_2 channel, constitute the input signal of the AND gate device. Fig. 1b shows an optical image of the AND gate device. The two parallel metals are the source electrode and drain electrode. Actually, the two vertical metals in Fig. 1b are fabricated under the channel and dielectric, so we call them the buried gates. Fig. 1c is the atomic force microscope (AFM) image. In this device, the thickness of MoS_2 is 4.3 nm, corresponding to 7 layers [37]. The 2D crystals were first confirmed by Raman force microscopy, shown in Fig. 1d. Two distinct peaks appeared around 383.5 and 406.6 cm^{-1} in several layers of MoS_2 crystal, corresponding to the in-plane (E^1_{2g}) and vertical (A_{1g}) vibration models. The Raman shift data is consistent with previous reports [38,39].

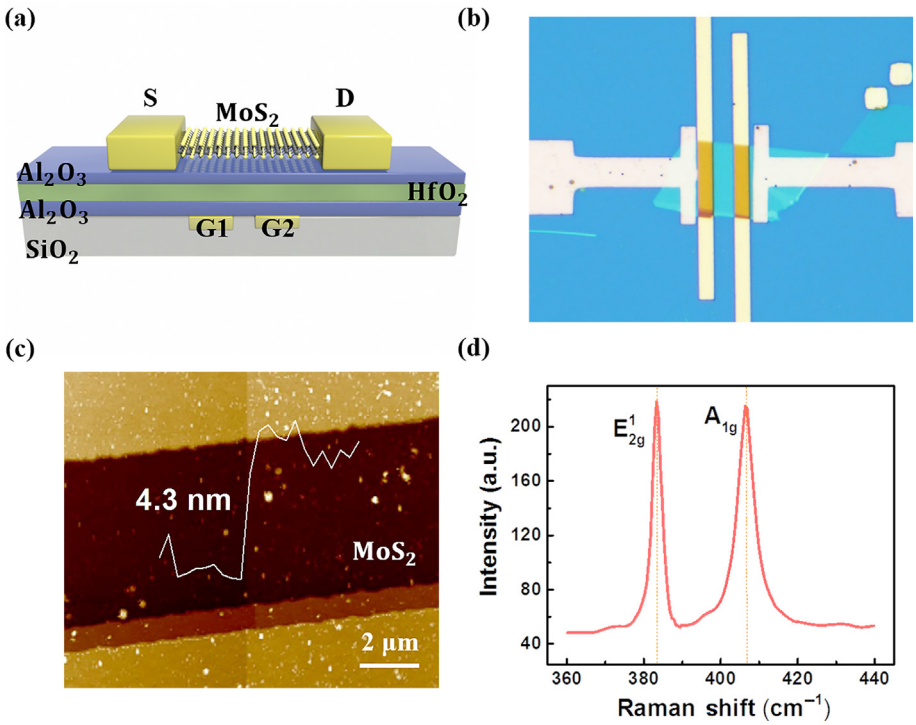

Fig. 1. (Color online) Characterization of the non-volatile AND gate device. (a) Schematic illustration of the device. (b) Optical microscopy image of the typical MoS_2 non-volatile AND gate. Two horizontal metal electrodes serve as source and drain, respectively. Two vertical metal electrodes serve as two separate buried gates as the logic inputs. (c) Atom force microscopy image of the device. The thickness of the MoS_2 is 4.3 nm. (d) Micro-Raman spectra performed on several layers of MoS_2.

Fig. 2a shows the basic dual-sweep transfer curve of the non-volatile AND gate device, indicating that each of the two separate buried gates has a basic memory characteristic. As for input G_1, the dual-sweep transfer curve shows a large threshold voltage window of approximately +3.3 V by sweeping gate voltage (V_{G1}) from −6 to 6 V, and back to −6 V. Meanwhile, the channel current is monitored by fixing source and drain bias to 0.5 V. Input G_2 is symmetric with G_1, indicating that the different parts of the MoS_2 controlled by corresponding buried gates have the symmetric memory performance. Fig. 2b demonstrates the memory operations of the first input gate (G_1).

The initial channel state is high-current under the reading voltage V_{G1} = −2 V. When a negative voltage pulse is applied to the input buried metal gate (G_1), a large current of about 1μA is observed in the channel by fixing source-drain bias at 0.5 V, indicating the device is set to a "1" state. When a positive voltage pulse is applied to the input G_1, a very small current under 10 pA is observed with V_{DS} = 0.5 V, indicating that the device is set to a "0" state. The same phenomenon can be observed by applying voltage pulses on the second buried metal gate with the same memory operations (Fig. 2c). The device shows the ratio of programmable current state ("1" state) and erasable state ("0" state) reaches about 10^5. Here, we briefly summarize the mechanism of the memory operations. With the positive pulse applied to the buried gate, electrons in the MoS_2 channel tunnel through the thin tunneling dielectric layer Al_2O_3 and are stored in the charge-trapping layer HfO_2. This causes the threshold voltage of the channel to shift right. After the pulse is removed, a very small current can be observed because of the right-shifting threshold voltage in the channel. When a negative voltage pulse is applied to the buried gate, electrons in HfO_2 would tunnel through the tunneling layer and return to the channel due to the negative electrical stress. And this causes the threshold voltage of the channel to shift left. A very large current state would be monitored under reading condition (V_G = −2 V, V_{DS} = 0.5 V) after the pulse is removed.

The logic AND characteristic is demonstrated in Fig. 3. Considering the two inputs of the logic AND gate, positive (+6 V) and negative (−6 V) voltage bias applied to the two separate buried gate

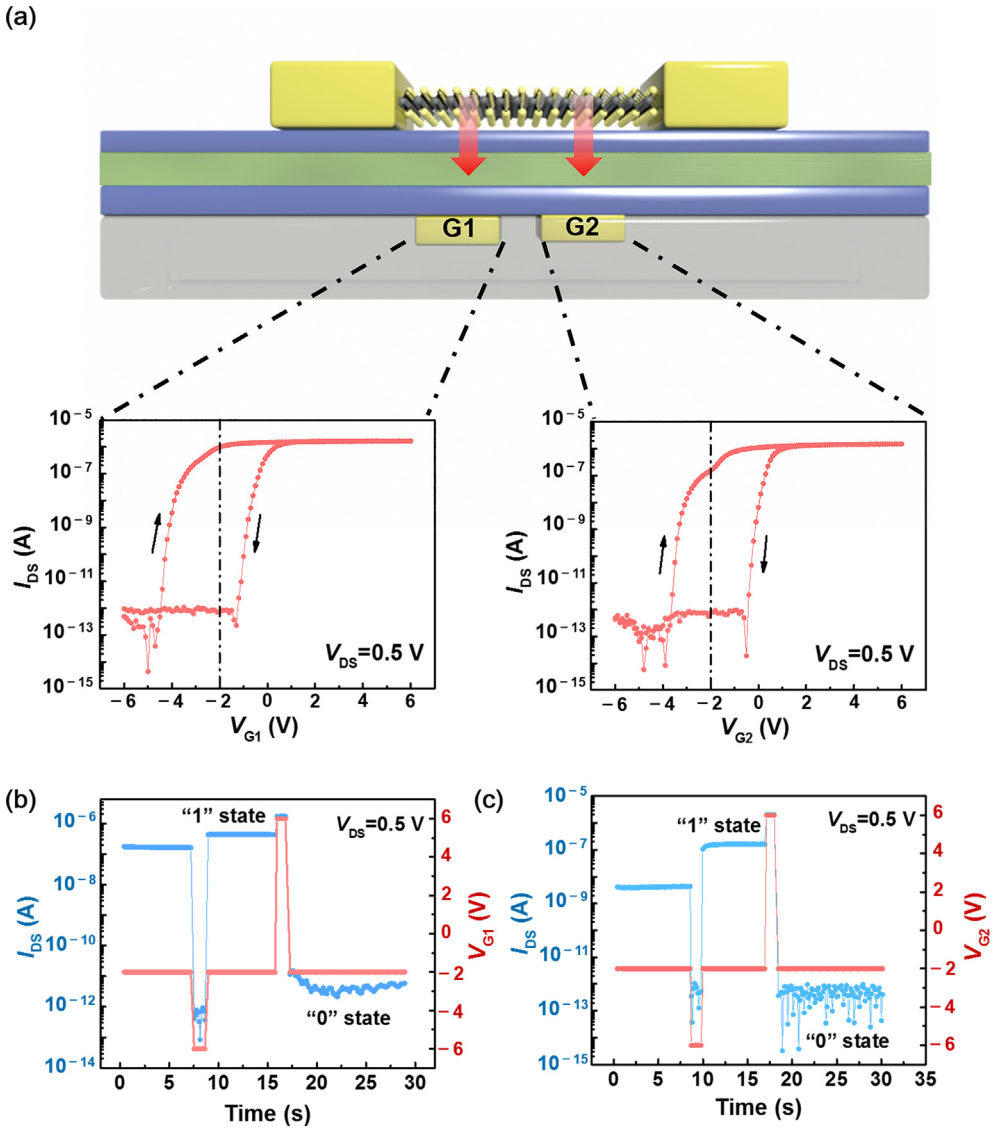

Fig. 2. (Color online) Basic memory performance of the device. (a) Transfer curves controlled by two separate buried gates. The bias voltage (V_{DS}) is 0.5 V during the test. The two parts of the transfer curve show the device has a good symmetry characteristic between the two gates. (b) The memory operation measured with V_{G1} when V_{G2} is open circuit. The reading condition: V_{DS} = 0.5 V, V_{G1read} = −2 V. The state-1/state-0 current ratio of the device can exceed 10^5. (c) The memory operation measured with V_{G2} when V_{G1} is open circuit. V_{DS} = 0.5 V, V_{G2read} = −2 V. The state current difference can also exceed 10^5, which shows a good symmetry characteristic between the two buried-gate transistors.

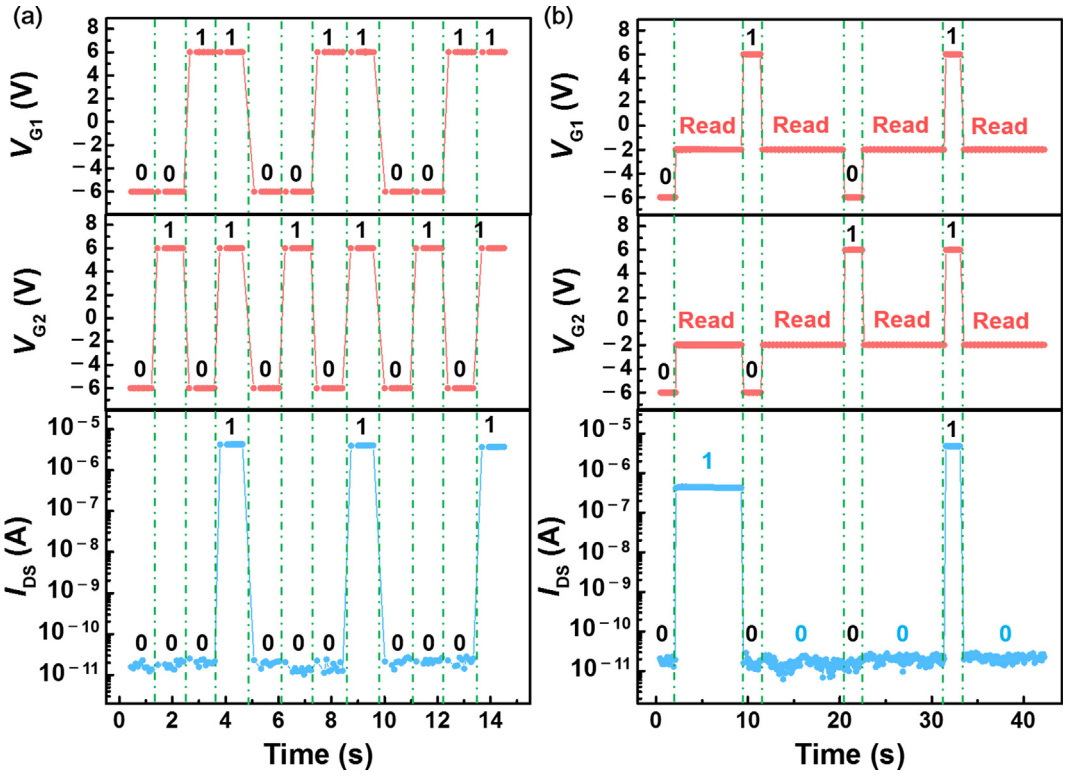

Fig. 3. (Color online) Logic and logic-memory performances with two separate buried gates serving as logic inputs. (a) Logic operations of the device. The device output characteristic exhibits a good AND gate logic. (b) Logic and memory operations of the device. The logic input pulses are applied firstly and followed by reading condition: $V_{G1read} = V_{G2read} = -2$ V, $V_{DS} = 0.5$ V. The output current state shows the logic-NOR characteristic during reading condition.

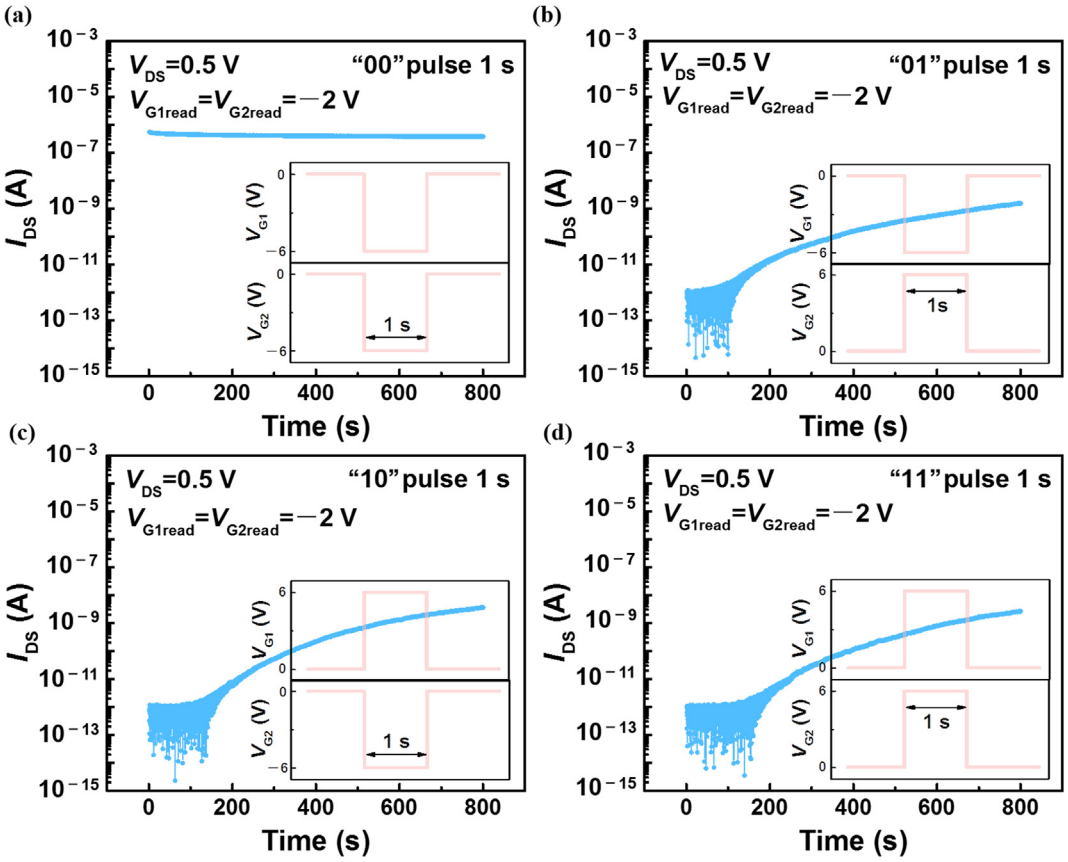

Fig. 4. (Color online) The non-volatile characteristic of the device after logic and memory operations. (a), (b), (c) and (d) show the retention diagrams of output state after "00", "01", "10", "11" logic operations, respectively. The pulse widths of the four logic input voltage pulses are all 1 s. The four states of the output current are measured at $V_{G1read} = V_{G2read} = -2$ V, $V_{DS} = 0.5$ V. There is still two orders of magnitude difference between "0" state current and "1" state current after 800 s, indicating the device has a non-volatile characteristic.

function as logic "1" and logic "0", respectively. The channel output current is chosen as the output signal. As shown in Fig. 3a, the alternant changing of the voltage bias of the two separate buried gates can simulate the different inputs of the logic AND gate. Firstly, negative voltage bias (−6 V) was applied to the two inputs of the device, indicating that the two inputs of the AND gate are "00". Obviously, the channel output current is below 100 pA, indicating that the logic output is "0". Similarly, when the input signals of this device are "01" or "10", the channel output current can also be at "0" state. Only when two positive voltages were applied to the two separate input electrodes, was a large current above 1 μA observed in the output channel, indicating that the channel output was at "1" state. The logic operations show our device has a good AND gate characteristic. Furthermore, the dielectric of our

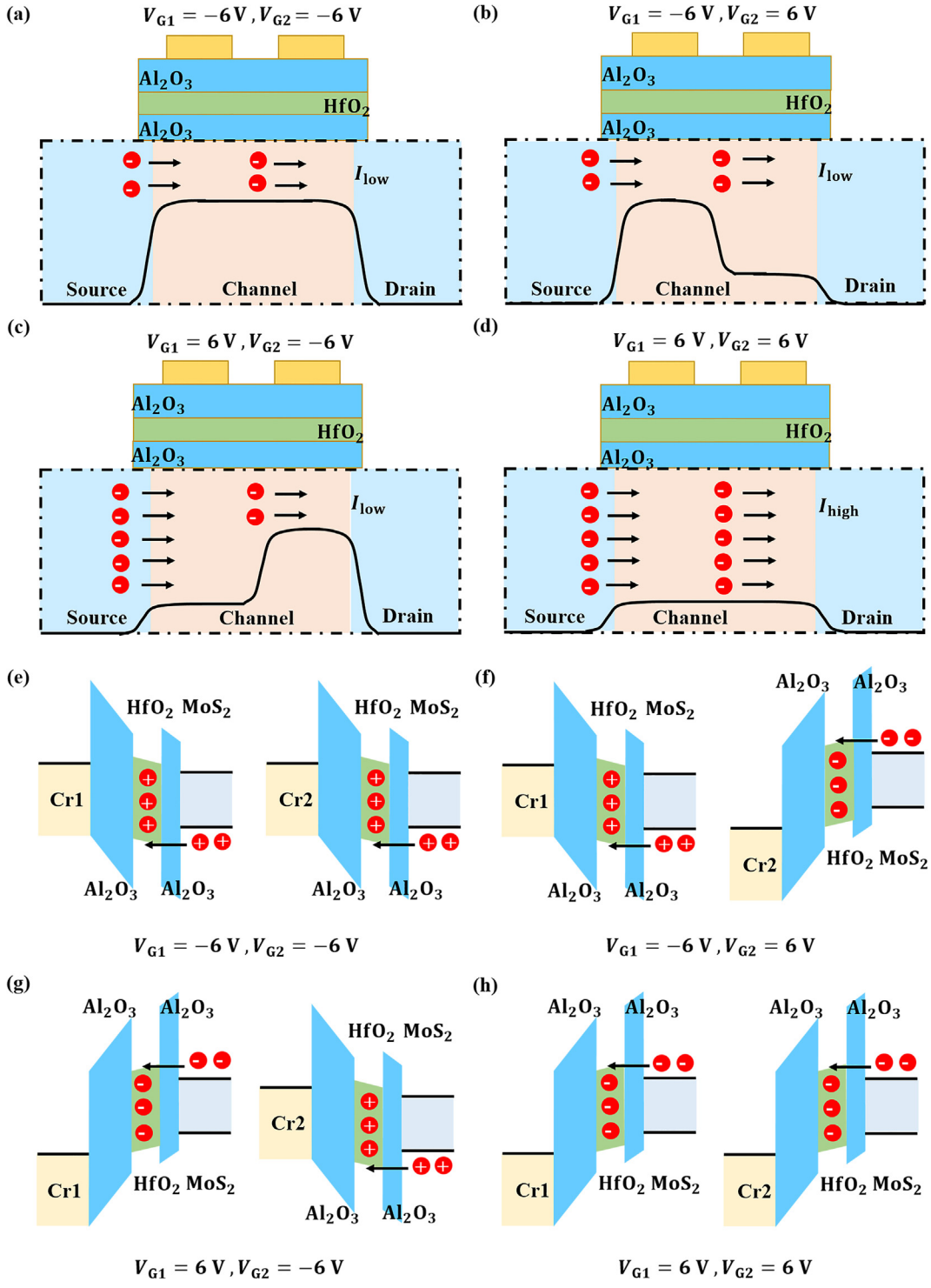

Fig. 5. (Color online) Schematic illustrations of the mechanism of the non-volatile AND gate device under two different operations: logic operations and logic and memory operations. Parallel energy band diagrams of the channel from source to drain at four different logic operations: (a) logic "00" operation, (b) logic "10" operation, (c) logic "01" operation, and (d) logic "11" operation. Different gates control the corresponding portions of the channel energy bands. Vertical energy band diagrams of the device under four different logic and memory operations: (e) "00" logic pulse operation, (f) "01" logic pulse operation, (g) "10" logic pulse operation and (h) "11" logic pulse operation.

device is composed of AHA heterostructures, which is capable of charge storage. Fig. 3b shows the logic operations and state reading process. After logic operations are performed on the device, the output state of the channel can be stored because of the AHA heterostructures. Followed by the reading process ($V_{G1} = V_{G2} = -2$ V), the state after logic operations can be obtained. After completing the logic "00" operation, the channel current shows a large current of about 400 nA. After proceeding with the logic "01", "10", "11" operations, the channel current is below 100 pA. Obviously, the stored state is different from the logic AND output, exhibiting a NOR logic characteristic. The stored-logic characteristic is demonstrated in Table S1 (online). In this case, the channel current will be set to high state after the negative pulse applied to the buried gate, which is proceeding the write-1 operation. Similarly, the channel current will be set to low state after the positive pulse is applied, corresponding to the erase-0 operation. This is mainly because the hysteretic transfer curve in this device is clockwise.

Fig. 4 shows the data retention abilities of the AND gate output states. After "00" operation, the output channel current is at "1" state during the reading operation ($V_{G1} = V_{G2} = -2$ V). As shown in Fig. 4a, the output state after "00" voltage pulse operation can be stored for at least 800 s. Fig. 4b, c and d show the data retention ability after "01", "10", "11" operations, respectively. The channel output current is below 1 pA at the beginning of the reading operation. After 800 s, there are still two orders of magnitude difference between the "1" state current and the "0" state current, indicating that the device has good data retention ability. In addition, the voltage pulse applied to the separate gate is only ±6 V, which is much lower than that in reported 2D flash memory devices [22,40,41], indicating that this device has great potential to reduce power consumption and cross-line interference. The fatigue resistance of this device is shown in Fig. S2 (online). The state current can still be read after 50 cycles of logic AND operations.

The conduction characteristic of conventional field effect transistors is completely dependent on whether electrons can cross the electronic barrier and move from the source to the drain [42]. The dual buried-gate non-volatile AND gate shows the separate controlled electronic barrier which determines the channel current in the device. Fig. 5a shows the "00" operation mechanism of the non-volatile AND gate. When $V_{G1} = V_{G2} = -6$ V, two separate parts of the barrier in the channel will rise synchronously, which will cause fewer electrons to move from the source to the drain. So, the logic operation output of the device is "0" when applying the "00" logic operation bias. When the "01" or "10" logic operation is applied on the two separate buried gates, one part of the channel barrier will rise which is under the control of negative bias and the other part of the barrier will drop which is under the control of positive bias. Since the two buried-gate transistors are connected in series, as shown in Fig. 5b and c, the electrons cannot move over the barrier even though there is a lower barrier in one part of the channel. As a result, when "01" and "10" logic operations are applied, the output channel current is still at "0" state. Only when the two separate buried gates apply positive bias ($V_{G1} = V_{G2} = 6$ V), do the two parts of the channel barriers drop, and electrons can easily move from the source to the drain over the low barriers (Fig. 5d). In this case, the channel output current is at "1" state. The logic operations indicate that the device has a good logic AND characteristic. When logic and memory operations (using logic-input pulses and reading operations to monitor the output state) are applied to the buried gates, the channel output states present logic NOR characteristics. Fig. 5e–h show the energy band mechanism diagrams of four different logic and memory operations. The reading operation is $V_{G1} = V_{G2} = -2$ V, $V_{DS} = 0.5$ V. As shown in Fig. 5e, when −6 V voltage pulses are applied to two separate buried gates, large numbers of holes in the separate parts of the channel tunnel through the tunneling layer Al_2O_3 and are stored in the charge-trapped layer HfO_2, which causes the threshold voltage to shift left. Therefore, a large current in the channel is monitored during the reading operation, indicating the output is at "1" state. When applying +6 V voltage pulses to two separate buried gates, as shown in Fig. 5h, a large number of electrons tunnel through the tunneling layer Al_2O_3 and are stored in the charge-trapped layer HfO_2, which causes the threshold voltage to shift right. As a result, the channel output is at "0" state during the reading operation. As for "01" and "10" operations (Fig. 5f and g), the threshold voltage of one part of the channel shifts left and the other part shifts right, corresponding to one buried gate applying −6 V voltage pulse and the other applying +6 V. One part of the channel can output high current and the other outputs low current. Therefore, after the "01" or "10" logic and memory operation, one of the corresponding channel portions controlled by the two buried gates is in an off-state, so that the channel current continues to maintain the "0" state. The output of logic and memory operations indicates the device has a good non-volatile NOR characteristic.

4. Conclusion

In summary, combining the logic gate function of 2D electronic devices and the data storage capability of $Al_2O_3/HfO_2/Al_2O_3$ charge-trap gate stack, a non-volatile AND gate was developed. We explored the electrical performance of the non-volatile AND gate device from two aspects: logic operation and state storage. The logic operation test exhibits this device has significant current discrimination between the "0" state and the "1" state. The logic output shows an excellent logic-AND characteristic, which has an approximate 10^5 state-1/state-0 current ratio. Meanwhile, the output state can be stored after logic operations. And there are still two orders of magnitude difference between the "0" state and the "1" state current after 800 s, indicating that the device has a non-volatile memory characteristic. The function of integrating logic and memory in a single device offers more possibilities for in-situ memory applications, which will pave the way for breaking the "memory wall" problem at transistor level.

Conflict of interest

The authors declare that they have no conflict of interest.

Acknowledgments

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Author contributions

Peng Zhou managed the project and guided the research. Jingyu Li conceived and developed the concept. Jingyu Li and Heng Zhang designed and conducted the experiment. Heng Zhang carried the device fabrication and characterizations. Jingyu Li carried out the electrical measurement and analyzed the data. Jingyu Li wrote the manuscript and Yi Ding, Jiayi Li, Shuiyuan Wang revised manuscript. David Wei Zhang provided the measurement equipment and all authors have approved the final manuscript.

Appendix A. Supplementary material

Supplementary material to this article can be found online at https://doi.org/10.1016/j.scib.2019.08.012.

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