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News & Views

Van der Waals integration of 2D atomic crystals for advanced multifunctional devices

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Semiconductor heterostructures play a key role in the development of solid-state electronic and optoelectronic devices. They are generally realized via traditional epitaxial integration, namely two or more dissimilar materials, with matching crystal lattice, polarity and thermal expansion coefficients, are grown on the surface of each other. In recent years, along with the booming development of two-dimensional (2D) atomic crystals, an entirely new integration mode—van der Waals integration—has captured the world's attention (Fig. 1a). Its basic principle is straightforward: different isolated 2D crystals are vertically stacked and adhered together by weak van der Waals forces. Such reassembled products are generally referred to as van der Waals heterostructures (vdWHs). Compared with traditional integration, the advantage of van der Waals integration is its arbitrariness, namely any 2D atomic crystals can be integrated layer-by-layer in a desired stacking order, sample thickness, relative angles, and so forth. This considerable operating controllability, coupled with the rich variety of 2D layered materials, offers a versatile material platform to probe new physics and device functionality. Moreover, the dangling-bond-free surface and strong in-plane covalent bond of 2D layers can effectively prevent atomic inter-diffusion at the hetero-interface, which is an undesirable process that degenerates the quality and working life of heterostructure devices.

On account of feasible band-structure engineering and high compatibility with the matured silicon-based microfabrication techniques, almost all the device types utilized in modern semiconductor industry, such as p-n junction and metal-oxidesemiconductor capacitor, can be realized with 2D vdWHs. However, with any new techniques, the early-stage studies related to heterostructure devices were mainly focused on the proposals of new device concepts. Steady improvement in device functionality and performance is highly desired to satisfy the requirements of practical application. And one challenge is how to integrate various high-performance electronic components into a single device, for it can offer higher integration level and overall energy efficiency. It is well known that device configurations have crucial importance in determining the device electrical properties. Thus, in the following, we will briefly discuss the main properties of four typical device configurations, which are classified by the relative locations of metal contacts and two semiconductor layers (i to iv in Fig. 1b).

The most basic one is hetero-bilayer sandwiched vertical structure (i), in which carriers transport direction is perpendicular to the atomic layers. This kind of device always exhibits very high output current density due to the ultrashort transport path, but the weak current modulation capability hinders its extensive use in diode and transistor. Since its electrical properties are mainly dominated by Schottky barriers at metal-semiconductor interfaces and band-offset between two semiconductors, introducing asymmetric metal contacts or increasing the corresponding band-offset could be an effective strategy to reduce the off-state current. When vertical heterostructure is connected in series with one or two extended lateral channel (ii, iii), its electrical properties are superimposed by heterostructure vertical transport and extra individual lateral transport. This configuration has benefits of abundant electrical transport behaviours, high current tunability and ultralow off-state current. However, it has drawbacks of low output current density. Considering that ultrathin 2D semiconductor owns superior immunity to short channel effects, thus, developing new fabrication techniques, such as scanning probe lithography and self-alignment electrode, to minimize the lateral transport length as much as possible has been regarded as a promising direction. Another configuration variant is hetero-bilayer lateral structure (iv), which can combine the channel characteristics of each constituent layer. For example, when n- and p-type semiconductors are composed together, the created dual-channel device will exhibit ambipolar behaviours. Not only that, due to the strong coupling between neighbouring crystal layers, numerous exotic physical phenomena, such as moiré superlattice effects and excitons transport, have been observed in a series of dual-channel vdWHs. For it owns fundamentally different properties from those of individual layers, this ultrathin hetero-bilayer structure also can be considered as an artificial metamaterial.

Recently, we reported the construction of high-performance, multifunctional devices by designing an asymmetric vdWH with graphene, h-BN, MoS_2 and $MoTe_2$, which can integrate diode, photodetector, PV cell, transistor and non-volatile memory (Fig. 1c) [1]. $MoS_2/MoTe_2$ junction (configuration ii shown in Fig. 1b) serves as

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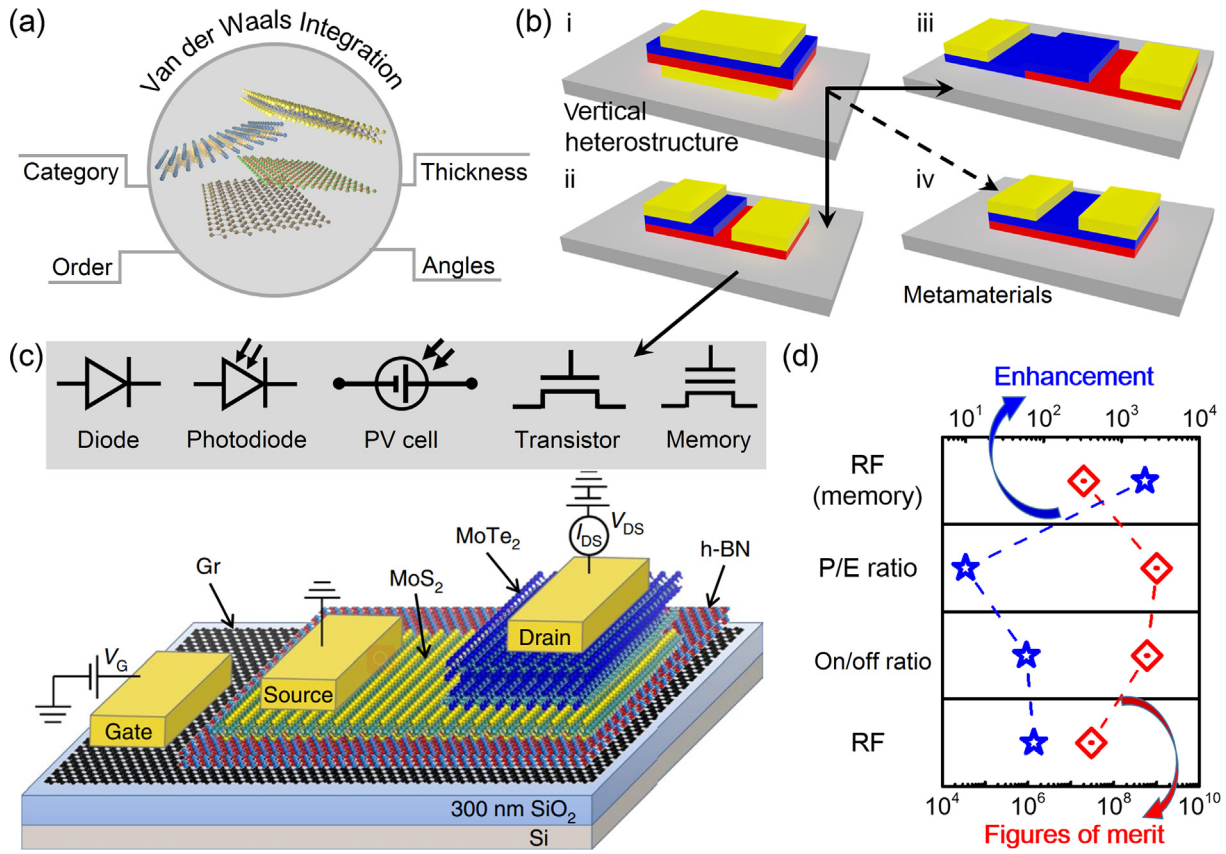

Fig. 1. (Color online) Van der Waals integration of 2D atomic crystals for improved device functionality and performance. (a) vdWHs can be created by integrating various 2D atomic crystals through selected category, stacking order, thickness and angles. (b) Four basic types of device configurations based on vertical heterostructures. Grey, yellow, blue and red box represent dielectric layer, contacts, top and bottom 2D atomic layers. (c) A three-dimensional (3D) structure schematic of $MoTe_2/MoS_2$/h-BN/graphene (Gr) heterostructure device, which can function as a diode, photodetector, photovoltaic (PV) cell, field-effect transistor and non-volatile memory [1]. (d) Some of device room-temperature figures of merit (curve with diamond), and their comparison with the current record ever reported for vdWHs (curve with star). RF: rectifying ratio for diode; on/off ratio: current on/off ratio for transistor; P/E ratio: program/erase current ratio for memory [1]. Copyright © 2018, Spring Nature.

the transport channel, and the voltage bias has been applied at the drain terminal. Enabled by the asymmetric structure of the device, the charge-carrier injection mode can be effectively controlled. That is, when applying a negative bias, the heterostructure has a severe band bending and the generated strong electrical field allows a considerable tunneling current to flow. Conversely, under positive bias conditions, the heterostructure goes back to a type-II band alignment and the transport mode is dominated by carrier recombination and thermal activation. As a result, the device exhibits very large current modulation capacity, allowing us to demonstrate multiple high-performance heterostructure devices. Some of device room-temperature figure-of-merit, including rectifying ratio (RF, for diode and programmable rectifier), current on/off ratio (for transistor), and program/erase current ratio (P/E ratio, for non-volatile memory), as well as their comparisons with the current record ever reported for vdWHs are displayed in Fig. 1d.

When graphene and h-BN are used as gate and dielectric materials, vdWH device functions as a standard field-effect transistor. Its current on/off ratio exceeds 6×10^8 for the ±3 V range of V_G, which can be attributed to the efficient gate tunability and reduced charge-carrier scattering. In addition, gate voltage exerts different regulating effects on the forward- and reverse-bias currents, resulting in a gate-controlled diode rectifying behaviours. At a specific gate voltage, the forward current can be completely shut off (~10 fA) for $V_{DS} = 3$ V. At the same time, the corresponding reverse current still remains at a high-current level (~μA). As a result, a record high rectifying ratio of $\sim 10^8$, which is two orders of magnitude higher than previous reports, is achieved. We also explored its photosensitive functions, such as photodiode, phototransistor and PV cell. On one hand, the device exhibits distinctive photocurrent behaviours under different bias conditions, further solidifying the proposed asymmetric carrier injection mechanism. On the other hand, its superior photodetection capabilities, including high photo on/off ratio ($\sim 4 \times 10^7$) and external quantum efficiency (7.522%), are also demonstrated.

Taking it a step further, we evaluated the performance of our device as non-volatile memory and programmable rectifier, for the reason of reducing circuit complexity and power consumption. Accordingly, graphene and h-BN serves as a charge-storing floating gate and a tunneling layer, respectively. Due to the tunable Fermi level of graphene, the number of stored electrons, which determines the memory states of device, can be effectively controlled by back-gate voltages. After applying a positive (negative) voltage pulses to the silicon substrate, the floating gate will exhibit a negative (positive) electrostatic gating effect, corresponding to the program (erase) state. Benefiting from the excellent current modulation capacity of our asymmetric structure, the device, when functions as memory, exhibits large memory window, low-power consumption and stable retention characteristic, as well as a record high program/erase current ratio (10^9, one order of magnitude higher than previous reports) and a record high non-volatile rectifying ratio (2×10^7, three orders of magnitude higher). More importantly, the capability of continuously tunable memory states, which is crucial to realize multi-bit storage and high-density integration, is also demonstrated by applying different voltage pulses and durations. The coexistence of memory and logic functionality

could provide a valuable direction toward future in-memory computing.

We have also explored one of its inverse structures: MoS_2 is engineered as a vertical channel sandwiched between the lateral $MoTe_2$ channel and a metal electrode [2]. Compared with the device configuration discussed above, quite different electrical and optoelectronic properties were observed even with same channel materials. One of the most notable features is dynamically-controlled conduction polarity. The corresponding semi-vertical transistors can be switched between unipolar and ambipolar just via altering the voltage bias. Moreover, when the device operates as ambipolar phototransistor, it can effectively suppress the trap states-related negative photoresponse effect that is widely observed in single ambipolar materials.

In summary, van der Waals integration brings us unprecedented convenience and innumerable possibilities in designing and creating semiconductor heterostructures. We have discussed the effect of device configurations on the properties, and shown that an asymmetric vdWH device owns extraordinary performance and unique functionality. With the emergence of novel device configurations and constantly improved assembly techniques, van der Waals heterostructures could play a larger part in future semiconductor industry.

Conflict of interest

The authors declare that they have no conflict of interest.

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