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Review

Interface engineering for two-dimensional semiconductor transistors

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ABSTRACT

Benefiting from the atomically thin body thickness of two-dimensional (2D) materials, field-effect transistors with 2D semiconductor as active channel enables enhanced electrostatic gate coupling for next-generation nanoelectronics. On the other hand, due to the atomic thin body and delicate lattice of 2D material, high-quality interfaces are essential to preserve the superior performance of the transistors, which is recognized as a key challenge within dangling-bond free 2D surface. Herein, we review and highlight recent state-of-the-art advances on interface engineering of high-performance 2D materials transistors, including contact engineering, dielectric engineering, surface charge transfer doping engineering, and intercalation engineering, and outlook the opportunities and challenges for developing 2D materials for low-power, high-performance microelectronics.

Contents

1 Introduction

Silicon (Si) based semiconductor technology has presented a dramatic exponential growth and been widely applied in our daily life. By scaling down the characteristic node of transistors, the number of transistors integrated (on single chip) is exponentially increased and the operation speed becomes ever faster. So far, a modern microprocessor and a typical memory contain more than 10 billion transistors, with gate lengths down to 10 nm and

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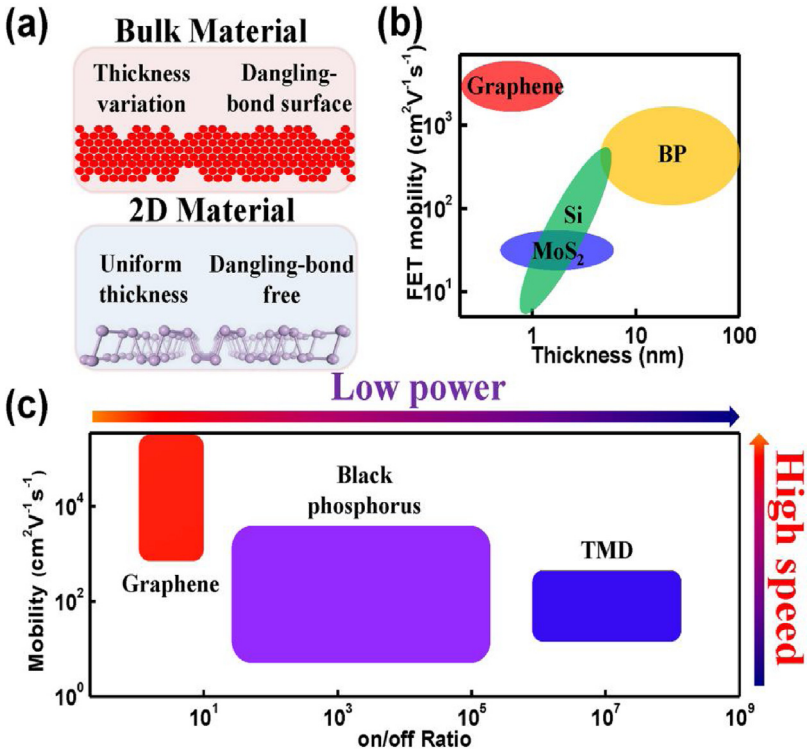

Fig. 1. (a) Schematic illustration of bulk materials and 2D materials. Reprinted from Ref. [17] with permission by Springer Nature. (b) The field effect mobilities of Si and typical 2D materials as a function of body thickness. (c) on/off ratios versus typical mobility values for 2D materials.

cost under 10^{-9} dollar [1–4]. The continuous miniaturization of field-effect transistors (FETs) promotes the progress of electrical requirement, which is governed by Moore's law [5,6]. Although continuous scaling down can provide performance improvement with the channel length (L_{ch}) down to sub-10 nm right now, short-channel effect (e.g. large off-state leakage current, high power consumption) dominants the carriers transportation in the channel and the device fabrication processes encounter technological problems (e.g. parasitic, strains, and lithography limitations) with further aggressive scaling [7–9]. As a consequence, International Technology Roadmap for Semiconductors (ITRS) suggests the More than Moore strategy: instead of aggressively scaling silicon electronics, continuous performance improvement is expected to be retained by the incorporation of newly discovered materials, and/or the application of new transistor concepts [10,11]. Therefore, it is highly desired to discover new semiconductor materials which could go beyond the limits of traditional Si electronics to meet the demand of the future nanoelectronics market. In 2004, graphene, as the first discovered two-dimensional (2D) material, opened up a new field of 2D FETs with its unique electrical, optical, mechanical, and thermal properties [12,13]. Since then, a variety of 2D materials such as transition metal dichalcogenides (TMDs) [14–16], black phosphorus (BP) [17] and hexagonal boron nitride (hBN) [18] have been extensively investigated for their intrinsic properties. Such materials are built up by out-plane van der Waals force and can be mechanically exfoliated into a monolayer with typical thickness below 1 nm. Compared with traditional bulk materials, 2D materials are atomically thin and have a naturally uniform and dangling-bond free surface (Fig. 1a), indicating the capacity of aggressively scaling for the next generation transistors [3,19–21]. In addition, Si shows a substantial degradation of carrier mobility with decreasing body thickness below 10 nm, presenting a critical scaling limitation to ultra-thin body thickness for the sub-10 nm or sub-5 nm channel FETs [22]. In contrast, 2D materials, such as graphene [23], molybdenum disulfide (MoS_2) [24], and BP [25], exhibit a negligible change in this regime and promise relative high values, demonstrating the potential for next generation high performance and low power nanoelectronics (Fig. 1b).

To further understand the electrical feature of 2D materials, the mobility and on/off ratios of representative 2D materials are shown in Fig. 1c. Graphene exhibits excellent conductivity and ultra-high mobility of up to 220, 000 cm^2 V^{-1} s^{-1} at room temperature, which is one of primary motivations for its applications nanoelectronics [12,26–31]. However, due to the lack of bandgap, the ultra-small on/off ratio (typically below 10) greatly limits its application for logic transistors [32–35]. Although some approaches have been developed to open a bandgap in graphene, such as graphene nanoribbon [36], graphene nanomesh [37], dual-gated bilayer graphene [38] and hydrogenation graphene [39], they all involve mobility degradation and/or poor stability issues. In contrast, TMDs typically have appropriate band gaps ~1–2 eV, exhibiting a high on/off ratio exceeding 10^8, and can be assembled into a low power consumption transistor. However, the field-effect mobility at room temperature is typically below 100 cm^2 V^{-1} s^{-1}, greatly limiting its practical application for high performance transistors [14,40–46]. Therefore, the research focus is shifted to other high mobility and sizeable bandgap 2D materials, including BP. As an ambipolar semiconductor with suitable bandgap and relatively high mobility (~1000 cm^2 V^{-1} s^{-1}) [17,25,47–57], BP has a tunable polarity providing the opportunity to build complementary circuits, which is essential for practical application of logic functions. For any newly discovered 2D materials, their electronics performance, device fabrication process, and performance potential are major research topics. Owing to the naturally atomic body thickness, the performance of 2D devices is mainly controlled and determined by their interface properties [58,59], therefore, interface engineering plays an important role for device fabrication, including (a): 2D/metal interface, (b): 2D/dielectric interface, (c):

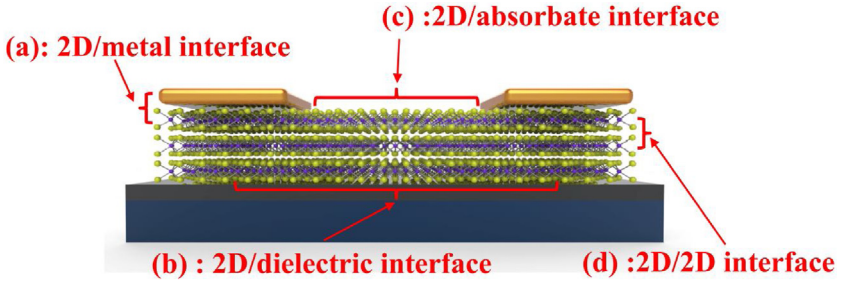

Fig. 2. Schematic illustration of the four interfaces in a 2D material based FET, including the 2D/metal interface, 2D/ dielectric interface, 2D/adsorbate interface, and 2D/2D interface, which are highlighted by the braces.

2D/adsorbate interface, and (d): 2D/2D interface, as displayed in Fig. 2. By optimizing the quality of interfaces, excellent intrinsic properties of 2D materials can be largely retained.

In this Review article, we focus on the interface of 2D transistors. We start from the contact barrier modulation at the 2D semiconductor/metal interface and classify several strategies of contact engineering strategies. Second, the dielectric engineering is discussed by providing various methods to improve the quality of 2D material/dielectric interface. Subsequently, a brief overview of doping at the 2D/adsorbate interface will be introduced, with a particular focus on the impact on electrical properties of 2D transistors. Finally, the homogenous interface of 2D transistors is discussed. By intercalation engineering, the changed 2D/2D interface brings intriguing effects on electronic properties without material damage.

2 Interface engineering

2.1 Contact engineering (2D/metal interface)

A typical transistor is composed of channel region and contact region. The total resistance (R_{tot}) of transistors comprises of channel resistance (R_{ch}) and contact resistance (R_c). As the channel length scaling down to sub-100 nm or even sub-10 nm regimes, the channel resistance quickly reduces and the contact issues are non-negligible. The contact barrier dominates the transistor performance, so it is essential to optimize the quality of the contact interface for high-performance FETs. In the following section, we mainly focus on the various approaches that have been employed to contact optimization of 2D FETs, discussing its merits and challenges.

2.1.1 Contact barrier

Typically, the contact barrier is mainly caused by the work function mismatch, which degrades the carrier injection efficiency from contact electrodes into the channel. The commonly-used contact barrier model is called Schottky barrier. The ideal Schottky barrier follows the Schottky-Mott rule [60,61], that is, the barrier height (φ_n) of given metal-semiconductor junction is the difference between metal work function (φ_m) and semiconductor electron affinity (χ):

$$\varphi_n = \varphi_m - \chi \quad (1)$$

Corresponding p-type Schottky barrier (φ_p) follows the equation

$$\varphi_p = E_g - (\varphi_m - \chi) \quad (2)$$

where E_g represents the bandgap of semiconductor. However, due to the existence of pinning effect at 2D/metal interface, the semiconductor/metal contact in practical applications rarely follows the Schottky-Mott rule. Instead, the Schottky barrier height is a combined effect of the Schottky-Mott rule and Fermi pinning effect. The metal Fermi level is pinned at the semiconductor interface state energy (φ_I) which does not coincide with the actual metal work function, as noted first by Bardeen [62,63]. The Schottky barrier equations are slightly corrected as

$$\varphi_n = (S \times \varphi_m - \chi) + (1 - S)\varphi_I \quad (3)$$

$$S = \partial\varphi_n / \partial\varphi_m \quad (4)$$

where S is the Schottky pinning factor. If S = 0, strong pinning effect dominate the junction properties and the Schottky barrier height is independent of the metal work function. If S = 1, the Schottky-Mott rule governs the barrier height and the barrier value can be well-controlled.

2.1.2 Traditional contact

Traditional contact in transistors always employs the metal deposition process that the metal is directly evaporated onto the contact region of 2D materials, resulting in non-van der Waals junction interface [64]. Thus, traditional contact enhancement is usually based on non-van der Waals junction interface.

As aforementioned, Schottky barrier is mainly determined by metal work function and semiconductor electron affinity governed by Schottky-Mott rule. By using suitable work function metal matching band edge (conduction band for n-type and valance band for p-type), the contact barrier as well as the contact resistance can be efficiently reduced and the electrical performance can be modulated. As shown in the inset of Fig. 3a, BP transistors with different metal contacts are fabricated [65]. Due to the tunable Fermi level of BP by gate electrical field, the R_c actually depends on the applied gate voltage, as shown in Fig. 3a. At low gate bias, the decrement of R_c results from the increase of carrier density in BP under the metal contacts. The high carrier density induced by the negative gate voltage enhances the carrier concentration in BP, leading to a narrower Schottky barrier width. Meanwhile, the narrowed Schottky barrier will facilitate the carrier injection from the metal into the valence band of BP, which leads to low contact resistance [66]. The R_c of Pd contacted device is $1.75 \pm 0.06\ \Omega \cdot$ mm at $V_{bg} = -40$ V, which is much smaller than the Ni contact resistance of $3.15 \pm 0.15\ \Omega \cdot$ mm at the same back gate voltage. This reduced contact resistance is mainly attributed to the different work function of the contact metals. Briefly, Pd contact with a work function of 5.4 eV will promise narrower Schottky barrier width in the contact region than that of Ni (with work function of 5.0 eV), thus the transistors exhibit better performance in term of on-state current and extrinsic mobility [65]. Fig. 3b shows the R_{tot} of Pt contacted BP transistor with different L_{ch} [67]. The contact resistance is extracted by the transfer length method (TLM) [33,42,66]. Different channel lengths are designed on the 2D material flake, and their R_{tot} of different channel lengths devices is extracted from $R_{tot} = V_d/I_d$. The total resistance includes both R_{ch} and R_c. The detailed equation is $R_{tot} = R_{ch} + 2R_c$. When channel length scales down to 0, R_{ch} is 0 and $R_{tot} = 2R_c$. Thus, the measured device resistance (R_{tot}) versus channel length is plot-

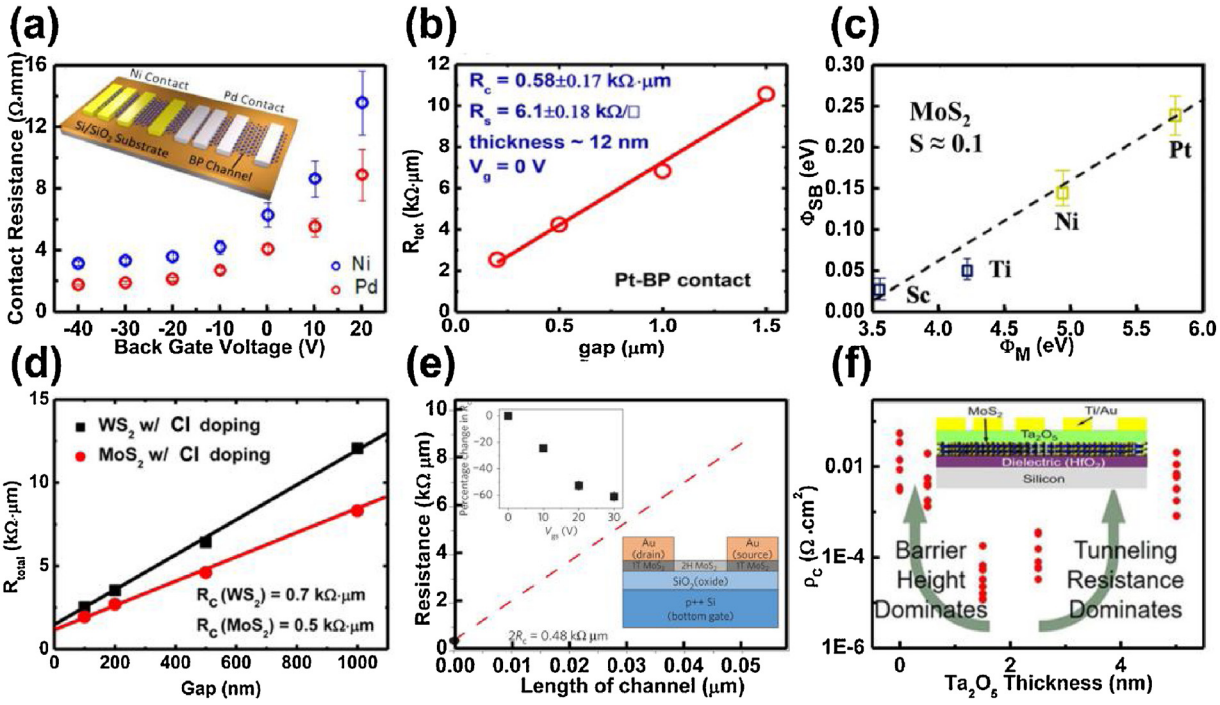

Fig. 3. (a) Contact resistance for both Ni and Pd contact metals at various gate biases. The inset is schematic view of device configuration. Metal contacts with various channel lengths from 3 μm down to 100 nm for both Ni/Au and Pd/Au are evaporated onto the same BP flake. Reprinted from Ref. [65] with permission by American Chemical Society. (b) Total resistance of BP FET with Pt electrodes as a function of channel length. Reprinted from Ref [67]. with permission by American Chemical Society. (c) Various Schottky barrier heights of MoS_2 FETs as a function of metal work function. Reprinted from Ref. [68] with permission by American Chemical Society. (d) Contact resistance for both WS_2 and MoS_2 with various channel lengths. Reprinted from Ref. [41] with permission by American Chemical Society. (e) Contact resistance of 1 T electrode MoS_2 FETs. The inset shows the percentage decrease in contact resistance with gate bias. Device schematics are also shown. Reprinted from Ref. [72] with permission by Springer Nature. (f) Measured specific contact resistivity ρ_c as a function of Ta_2O_5 dielectric thickness. The inset is side view schematic of MoS_2 transistors with Ta_2O_5 tunneling layer. Reprinted from Ref. [76] with permission by American Chemical Society.

ted, and the intercept determines $2R_c$. Through studying transistor behaviors with various channel lengths, the contact resistance is extracted to be a record low value of 0.58 ± 0.17 kΩ· μm, enabling a superior on-state channel current above 940 μA/μm. Additionally, a thorough comparison of contacts to MoS_2 using various metals, such as Sc, Ti, Ni, and Pt, is presented in Fig. 3c, with the metal work function ranging from 3.5 eV to 5.9 eV [68]. The Schottky barrier shows an obvious linear-dependent behavior as a function of metal work function. By Eq. (4), the extracted slope is ~0.1, which is far less than unity and shows a strong pinning effect at the MoS_2/metal interface. Hence, although the metal work function plays an important role in contact barrier, the pinning effect hinders the ideal scheme [68]. In addition, the high work function metals mostly are noble metals, while the low work function metal is easily oxidized and unstable [69,70], which increases the cost and further limits the benefit of metal work function modulation.

Hence, the research focus shifts from metal work function to the 2D material property modulation by doping the semiconductor. L. Yang et al. [41] report a novel chloride molecular doping method on 2D TMDs (Fig. 3d). The exfoliated MoS_2 or WS_2 flakes are soaked in undiluted 1,2 dichloroethane (DCE) at room temperature for more than 12 h. After doping, the contact resistance of MoS_2 and WS_2 are reduced to 0.5 kΩ· μm and 0.7 kΩ· μm, respectively. The n-type doping significantly reduces the Schottky barrier width, thus, the electron can be efficiently injected through the barrier into active channel, resulting in low contact resistance. Besides, dopant diffusion and ion-implantation approaches are also employed to improve the contact resistance [71]. However, these methods typically involve involuntary reliability and long-term stability issues of the fabricated devices or introduce defects in the 2D channel through the fabrication processes, limiting further development of 2D materials for integrated circuits.

Based on phase engineering, R. Kappera et al. [72] fabricate low contact resistance MoS_2 FETs with organolithium chemical method, by which the semiconducting 2H phase MoS_2 is convert to the metallic 1 T phase in the contact region (Fig. 3e). The insets of Fig. 3e are the percentage decrease in contact resistance with gate bias and device schematics. By locally patterning the metallic 1 T phase on 2H phase MoS_2 nanosheets as contact region, the contact resistance is reduced from 1.1 kΩ· μm to 0.24 kΩ· μm at zero gate bias, leading to on-state currents of 85 μA/μm, high mobility values of ~50 $cm^2\ V^{-1}\ s^{-1}$, subthreshold swing (SS) values of 95 mV/dec, and on/off ratios above 10^7. However, the 1 T phase is metastable, with relaxation energy of ~0.1 eV for conversion to the thermodynamically stable 2H phase [73–75], so the long-term stability remains to be further investigated under high-performance device operation.

Unlike the previously reported methods for lowering the contact resistance that rely on volatile chemistry approaches, an air-stable method with Ta_2O_5 as the tunneling layer to form a metal-insulator-semiconductor contact is adopted for lowering the contact resistance [76], as shown in Fig. 3f. This improvement is attributed to the attenuation of metal induced gap states and such MIS contacts approaches have been shown to reduce the Schottky barrier height of Si [77], Ge [78], and III-V materials [79,80]. In Fig. 3f, the inset is the side view schematic of the device structure. Various thicknesses of Ta_2O_5, ranging from 0 to 5 nm, are deposited by atomic layer deposition (ALD) technique and the specific contact resistivity (ρ_c) is extracted through TLM method. The contact resistivity shows a sharp degradation with the insertion thickness increasing, whereas ρ_c increases again as the Ta_2O_5 thickness over 1.5 nm. Within metal-insulator-semiconductor contact, the contact resistance is modeled as two parts: the resistance due to the Schottky barrier (R_{SB}) and the resistance due to tunneling through the insulator (R_T). As the Ta_2O_5 thickness is less than 1.5 nm, the R_{SB}

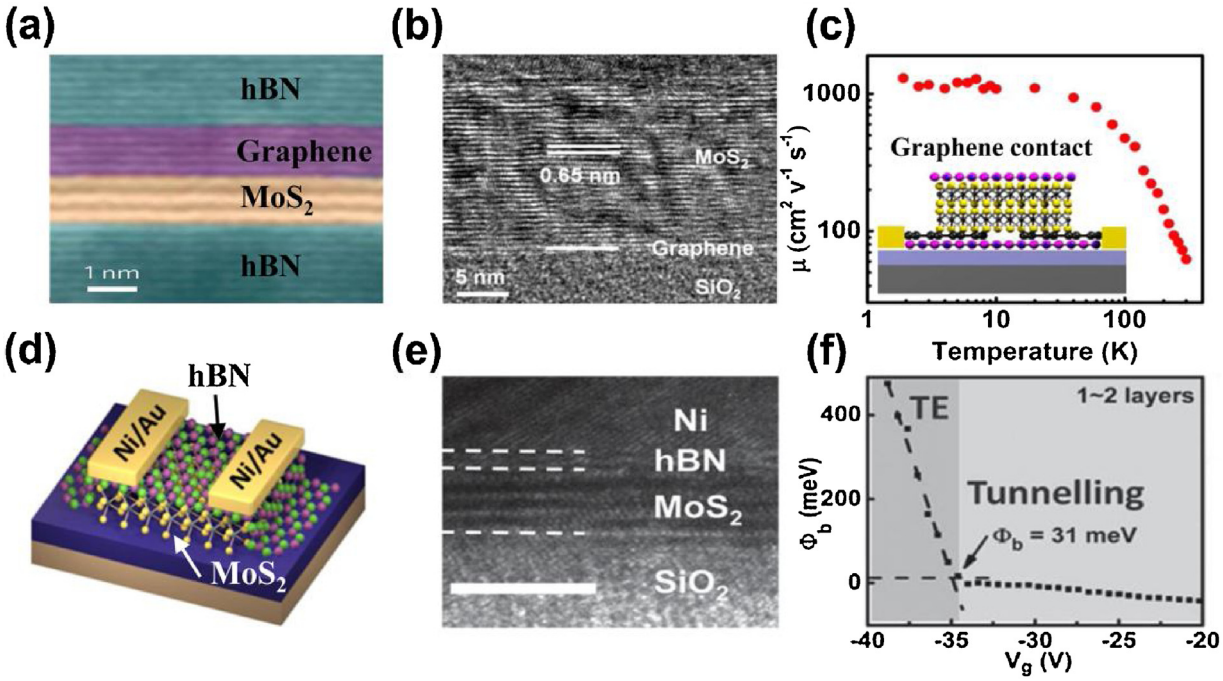

Fig. 4. (a) Cross-sectional STEM image of the fabricated device. The false-colour image shows the ultra-sharp interfaces between different layers (graphene, 5 L; MoS_2, 3 L; top hBN, 8 nm; bottom hBN, 19 nm). Reprinted from Ref. [85] with permission by Springer Nature. (b) Cross-sectional TEM image of the graphene-MoS_2 interface. (c) Field effect mobility of the device shown in the inset as a function of temperature, with the highest mobility over 1300 cm^2 V^{-1} s^{-1}. The inset is schematic illustration of a BN/graphene/MoS_2/BN sandwich structure with edge graphene contacts. Reprinted from Ref. [86] with permission by American Chemical Society. (d) Schematics of a MoS_2 FET with hBN tunneling layer contacts. (e) Cross-sectional HRTEM image of the interface between MoS_2 and hBN. The scale bar is 5 nm. (f) The Schottky barrier heights for different back gate bias when thickness of hBN are 1–2 layers. Reprinted from Ref. [42] with permission by John Wiley and Sons.

dominates the total contact resistance. The inserted thin insulator effectively lowers R_{SB} with a small added R_T, reducing the overall resistance. Once the insulator thickness is beyond 1.5 nm, R_T begins to dominate the total resistance, resulting in higher overall contact resistance. This work presents a feasible approach for lowering the contact resistance by introducing a tunneling layer between metal and 2D channel. Other insulators, such as TiO_2 [81,82] and MgO [83], also have been utilized as a tunneling layer to reduce the contact resistance. However, due to the dangling-bond free surface of 2D materials, quality and thickness control of the insulator tunneling layer should be improved to enhance the reproducibility and reliability of the fabrication processes.

2.1.3 Van der Waals contact

In the traditional metallization processes, the fabrication of metal electrodes typically relies on chemical deposition or physical deposition directly on 2D material surface with high-energy processes. These approaches are responsible for the damage, strongly local heating and interface disorder with the contact region [84]. Thus, there are many defects, diffusion, bonds and strain at the traditional 2D/metal interface (Fig. 5a and b), resulting in the Fermi level pinning. On the other hand, van der Waals contact uses the van der Waals heterogeneous integration technique that the contact material is indirectly fabricated onto 2D semiconductor without direct chemical bonding, avoiding the damage of the evaporation process and the diffusion at the contact interface [64].

An earlier strategy of van der Waals contact strategy is inserting 2D materials, such as graphene [85–91] and hBN [42,92,93], as the buffer layer to assemble a van der Waals contact in Fig. 4. The buffer layer is pre-fabricated and physically laminated onto 2D semiconductors to minimizing the damage during the high-energy metal evaporation. The application of graphene as the buffer layer has reduced the contact resistance between the metal and MoS_2. After inserting graphene into the MoS_2/metal interlayer, the strong chemical bonds between metal and MoS_2 is minimized and the generation of metal induced gap states is suppressed [94,95]. Furthermore, the Fermi level of graphene can be readily tuned by gate voltage to enable a perfect band alignment with MoS_2 for a finite density of states [68,96]. Meanwhile, graphene belongs to 2D materials that are atomically thin and dangling-bond free, resulting in an atomically flat interface. Fig. 4a shows a high resolution scanning transmission electron microscopy (STEM) image of the contact region [85]. The graphene overlaps the MoS_2 and extends to the edge, where it is in turn contacted by metal electrodes. The entire device is fully encapsulated and protected by hBN. Fig. 4a confirms that the interface is ultraclean and atomically flat without any damage on MoS_2. However, in such top contact (graphene on top of MoS_2) geometry, the underlaying MoS_2 could partially screen the gate electrical field [97], resulting in insufficient tuning of graphene Fermi level and undesired band-alignment. This challenge could be overcome through co-planer contact geometry by using graphene as the back electrodes, as shown in Fig. 4b and c [86]. The inset in Fig. 4c is the schematic of device structure. The entire device is also fully encapsulated and protected by hBN. Fig. 4b is a cross-sectional TEM image of the junction, indicating that the van der Waals contact provides a high quality interface to minimize the damage of MoS_2, reduces interface charge trapping states, and prevents Fermi level pinning. The graphene contact forms a barrier-free contact to MoS_2 and shows two terminal mobility of 1300 cm^2 V^{-1} s^{-1} at 1.9 K. However, because graphene is a semi-metal, the fabricating technology will be quite complex to avoid short out. Thus, hBN tunneling layer is used to reduce the Schottky barrier.

Benefiting from the atomic thickness of 1–2 layers hBN, the Schottky barrier can be greatly reduced with small tunneling resistance (Fig. 4d). The cross-sectional TEM image of hBN/MoS_2 contact is presented in Fig. 4e, demonstrating a uniform interface. Comparing with Fig. 3f, the insulator layer is natural uniform and atomically thin to minimize the series tunneling resistance [42]. At the same

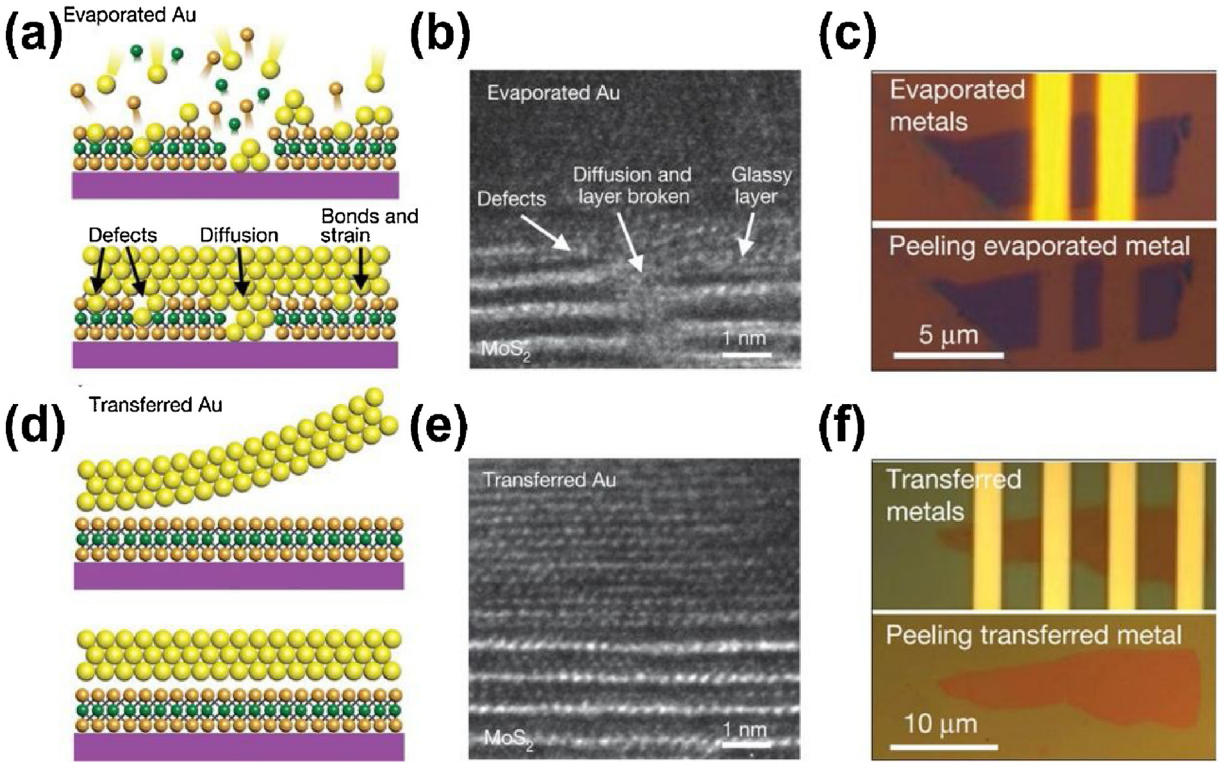

Fig. 5. (a–b) Cross-sectional schematics and TEM images of the transferred metal electrode on top of MoS_2. (c) Optical image of the MoS_2 device with transferred electrodes (upper) and with the transferred electrodes mechanically released (lower). (d–e) Cross-sectional schematics and TEM images of conventional deposited metal electrodes on top of MoS_2. (f) Optical image of the MoS_2 device with deposited electrodes (upper) and with the deposited electrodes mechanical released (lower). Reprinted from Ref. [64] with permission by Springer Nature.

time, the insertion of hBN separates metal from MoS_2 to protect the underlying MoS_2 and form a van der Waals contact. Owing to the improved tunneling contact, the transistor shows a small Schottky barrier of 31 meV, a high FET mobility of 73 $cm^2\ V^{-1}\ s^{-1}$, and output current of 330 μA/μm at room temperature, which can increase to 321.4 $cm^2\ V^{-1}\ s^{-1}$ and 572 μA/μm, respectively at 77 K. Similarly, Avsar et al. [98] apply Co/hBN contact to BP transistor, which exhibits low contact resistances (~4.5 kΩ) and high electron mobilities (4200 $cm^2\ V^{-1}\ s^{-1}$), indicating that hBN contact can be expanded to other 2D materials. Importantly, this van der Waals approach is compatible with the traditional fabrication process and the large-area chemical vapor deposition (CVD) grown technique, which would be important for the large scale integration.

To further research the ideal 2D/metal interface, metal electrodes are first prepared on a silicon substrate and physically transferred on top of MoS_2 flakes [99–102], exhibiting a representative van der Waals contact where the Schottky barrier approaches the Schottky-Mott limit [64,103]. The transferred MoS_2/metal interface presents an atomically sharp interface, which can be clearly seen in cross-sectional transmission electron microscopy (TEM) images (Fig. 5d and e). In contrast, the deposited MoS_2/metal interfaces show considerable defects, strain, disorder and metal diffusion during the transistor fabrication process (Fig. 5a and b). To demonstrate that the transferred integration approach preserves the pristine nature of the underlying material, the metal electrodes are mechanically peeled from MoS_2 after the device measurement. The MoS_2 under transferred metal electrodes shows a clean surface without any apparent damage (Fig. 5f), whereas the MoS_2 under deposited metal electrodes is destroyed by strong chemical bonding at the contact interface (Fig. 5c). The surface structure of MoS_2 is largely preserved during the transfer process. Additionally, the Schottky barrier heights of various metals are extracted as a function of the corresponding work functions. For deposited metal electrodes, the extracted S is 0.09, consistent with Fig. 3c with S 0̃.1, indicating strong pinning effect. In contrast, the fitted S of the transferred metal electrodes is 0.96, approaching the limit of the Schottky-Mott rule, confirming the Schottky barrier is strongly dependent on the metal work function.

2.2 Dielectric engineering (2D/dielectric interface)

Although 2D materials exhibit excellent electrical properties, the experimental values differ from the theoretical values. The possible reasons for the discrepancy between the experimental data and the theoretical prediction are the serious extrinsic scattering of carriers, including the Coulomb impurities, traps at the interface, defects, and remote surface optical phonons [85,104,105]. These extrinsic sources of scattering are mainly attributed to the 2D/dielectric interface and lead to low quality devices with low mobility. Hence, dielectric engineering is crucial for integrated circuit technology. Two types of 2D/dielectric interfaces are generally encountered in 2D transistor. First one is the substrate interfaces, where 2D materials stack on top of the back-gate dielectric through weak van der Waals force. Another one is top gate interfaces, which needs to fabricate uniform dielectric onto the 2D materials surface to achieve the capability to individually tune each device with a top gate.

2.2.1 Substrate engineering

SiO_2 have been widely used as the gate dielectric layer for fabricating 2D materials transistors, however, due to the Coulomb impurities, traps, defects, and remote surface optical phonons, the performance of fabricated transistors is not competitive with theoretical prediction [105]. Mobility of 150 $cm^2\ V^{-1}\ s^{-1}$ is obtained by transferring MoS_2 flake directly onto the pre-fabricated HfO_2 substrate, in which the scattering originated from the 2D/dielectric

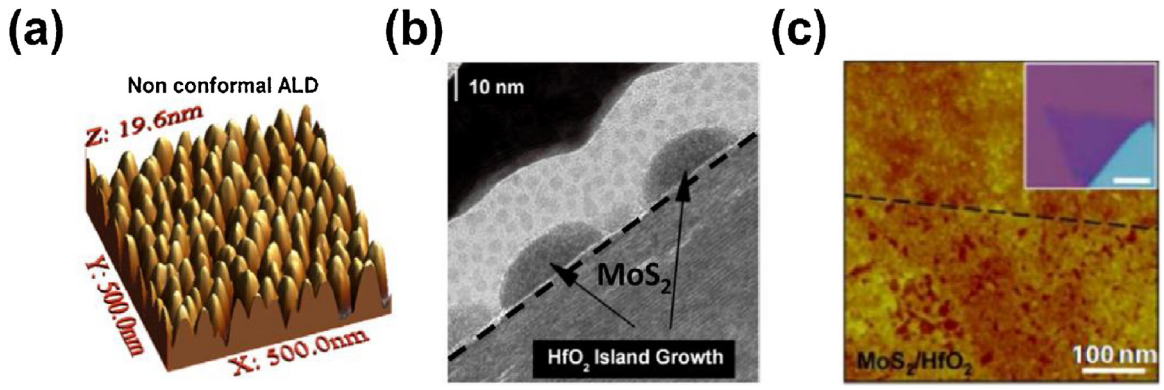

Fig. 6. (a) The 3D AFM image of HfO_2 deposited directly on MoS_2 by ALD technique forms an island structure. (b) The cross-section TEM image of (a). Reprinted from Ref. [110] with permission by American Chemical Society. (c) The AFM image of ALD HfO_2 on pristine MoS_2. The inset is optical image of MoS_2. Reprinted from Ref. [45] with permission by John Wiley and Sons.

interface is largely suppressed [106]. T. Li et al. [51] improve BP device performance by using the same way. Due to the low trap density and the effective screening of impurity scattering of HfO_2/BP interface, the mobility of BP transistor with HfO_2 as dielectric layer obtained a high mobility of 200 $cm^2 V^{-1} s^{-1}$, which is nearly a 100% enhancement when compared with the device with SiO_2 as dielectric layer. And the temperature-dependent Dirac point shift is also lower than that on SiO_2 dielectric substrate, indicating the improvement of 2D/dielectric interface. Besides, due to the high dielectrics constant, high-k dielectrics have thinner equivalent oxide thickness leading to enhanced electrostatic gate potential that modulates the channel materials [51]. Meanwhile, hBN [85,86], as an atomically smooth material, also can minimize the scattering and forms a sharp interface to optimize the transistor performance.

Except for conventional high-k dielectric, the novel ferroelectric $HfZrO_2$ [107] as a high-k insulator is also applied to minimize the SS of the MoS_2 transistors. The SS is obviously lower than 60 mV/dec with the ferroelectric dielectric acting as a negative capacitor. The device exhibits essentially hysteresis-free switching characteristics with a maximum drain current of 510 μA/μm, indicating a high quality interface. Similarly, X. Liu et al. [108] pull down the SS value of MoS_2 FETs to 42.5 mV/dec by introducing a layer of ferroelectric poly (vinylidene fluoride-co-trifluoroethylene) (P(VDF-TrFE)) in the gate dielectric stack. The negative capacitance effect of ferroelectrics can effectively break the Boltzmann limitation of SS ≥ 60 mV/dec.

2.2.2 Top gate dielectric interface engineering

To realize integration in 2D FET circuit for practical application and permit further device scaling, top-gated 2D FETs with high-k dielectric are indispensable. Although uniform high-k dielectric films can be deposited through ALD in the thickness of sub-10 nm, compact and conformal top-gated dielectric deposition directly onto the 2D materials still remains challenging for the dangling-bond free surface. As a result, ALD on pristine 2D materials often leads to the dielectric growth only on the surface with traps and impurities, and the island growth are typically observed [45,109,110]. Fig. 6a–c shows the Atomic Force Microscope (AFM) images and a cross-sectional TEM image of the ALD HfO_2 on the MoS_2 surface [45,110]. The inset of Fig. 6c is the original MoS_2 sheet optical microscope image. It is clear to see that the ALD film is non-uniform and very rough. The AFM images exhibit the formation of pinhole-like defects and the resulted film is not continuous and compact. Therefore, one primary task for high performance top-gated 2D transistor is to discover a high quality dielectric fabrication strategy. To keep the dielectric film conformal, two ideas are suggested. First, similar to van der Waals contact, the dielectric is pre-prepared and directly transferred onto 2D materials. Second, some dangling-bonds and functional groups are intentionally created on the 2D materials surface to act as the nucleation layer of ALD growth.

Transfer method is a van der Waals approach. The dielectric can be individually prepared and directly transferred onto the 2D materials, which perfectly overcomes the challenge of the ALD growth on 2D materials surface. In 2010, L. Liao et al. [31] first use free-standing Al_2O_3 nanoribbons to assemble a high performance top gate graphene FET (Fig. 7a). High quality Al_2O_3 nanoribbons are synthesized through physical vapor approach with high crystalline structure, as shown in Fig. 7b. The cross-sectional TEM image shows that the graphene layer is intimately integrated with the crystalline Al_2O_3 nanoribbon without any appreciable gap and impurities, suggesting that the physical assembly method can effectively integrate Al_2O_3 nanoribbon with graphene without introducing any obvious defects into the graphene surface, and thus can effectively preserve the high carrier mobility in the resulting devices [31]. By further evaluating the top-gated devices versus standard back-gated devices, the transfer characteristics of top-gated devices are similar to that of back-gated device (Fig. 7c and Inset). The maximum transconductance (g_m) of the top-gated device is about 290 μS, with an enhancement factor about 15 in contrast with the corresponding back-gated configuration (~19.5 μS). The corresponding mobility of the top-gated device can reach up to 23,600 $cm^2 V^{-1} s^{-1}$, which is consistent with the back-gated device. Using the Al_2O_3 nanoribbons as the gate dielectrics, the top-gated graphene transistors have been fabricated to exhibit superior performance with the highest carrier mobility observed in top-gated device to date. This method opens a unique avenue to integrate high-k dielectrics on graphene with the preservation of high carrier mobility.

The same year, based on the above paper, high-speed graphene transistors with a self-aligned nanowire gate is reported [111]. Instead of Al_2O_3 nanoribbons, a Co_2Si-Al_2O_3 core-shell nanowire is aligned on top of graphene flakes (Fig. 7d and e). The Co_2Si nanowires are synthesized by a CVD approach and the resistance of them is low enough to act as gate electrodes [112]. The 5 nm Al_2O_3 dielectric fully encapsulates the Co_2Si nanowire by ALD, which is uniform and conformal to avoid electric leakage. To reduce gate-source and gate-drain capacitance, self-aligned structure is formed by utilizing the height difference between the nanowire gate and the semiconductor channel [111]. Through using the nanowires (diameter ~100–300 nm) as a mask, the source and drain are well separated and precisely aligned next to the top gate after depositing a 10 nm Pt film. Graphene transistors with a channel length as low as 140 nm is formed and the gate control is enhanced, resulting in the performance improvement of the graphene top gate transis-

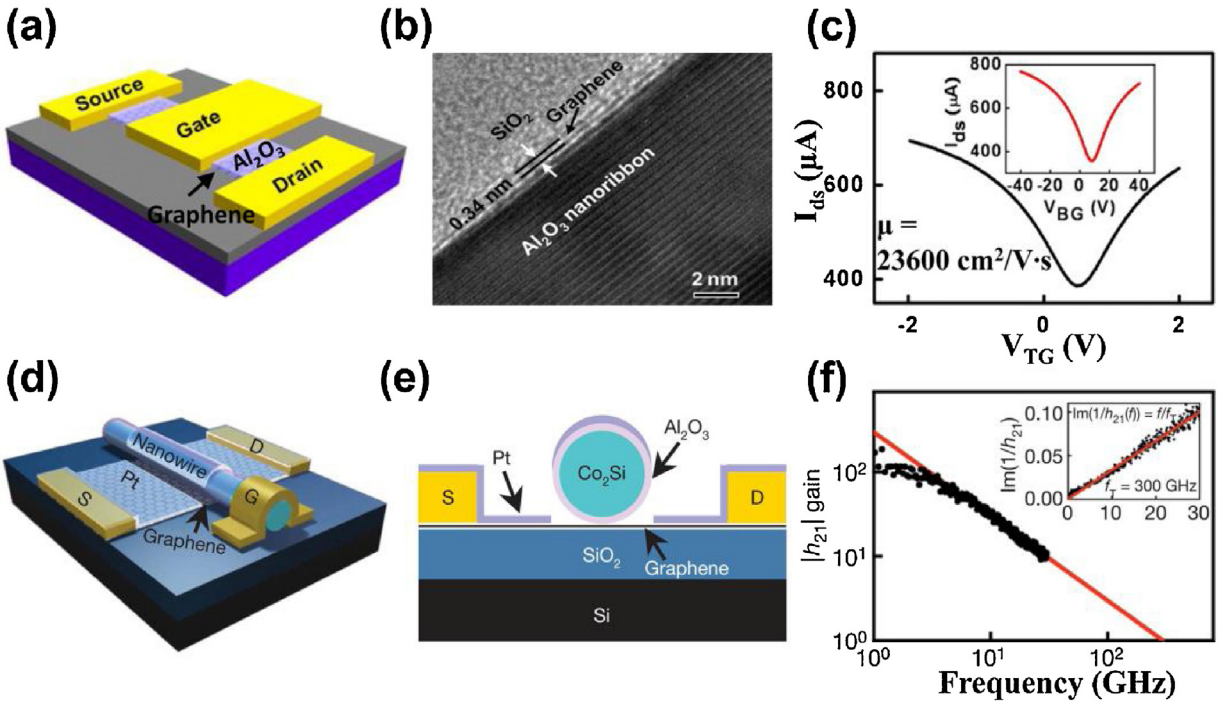

Fig. 7. (a) Schematic illustration of graphene transistors using dielectric oxide nanoribbons as top gate dielectric. (b) A cross-section HRTEM image of the interface between Al_2O_3 nanoribbon and a trilayer graphene. (c) Transfer characteristics for the device using top and back gate (Inset). Reprinted from Ref. [31] with permission by National Academy of Sciences. (d–e) Schematic illustration of a high-speed graphene transistor with a Co_2Si–Al_2O_3 core–shell nanowire as the self-aligned top-gate. (f) Measured small-signal current gain |h21| as a function of frequency f. Gate length of the graphene device is 144 nm. The inset shows the extraction of f_T by Gummel's method. Reprinted from Ref. [111] with permission by Springer Nature.

tor with the scaled on-current of 3.32 mA μm^{-1} and scaled g_m of 1.27 mS μm^{-1}. Meanwhile, as a radio frequency device, the high quality top gate graphene transistor exhibits a unprecedented cut-off frequency reach up to 300 GHz, which can catch up with the performance of InP and GaAs with similar channel length, indicating the potential of graphene in high speed electronics [113]. With this nearly perfect van der Waals approach, R. Cheng et al. [114] optimize the performance up to 427 GHz. Instead of using a nanowire, the gate stacks (Al_2O_3/Ti/Au) are built by processing conventional lithography, deposition, and etching steps on a sacrificial substrate. Then the top stacks are transferred onto graphene and as a mask to pattern the drain and source. These damage-free assemble process and self-aligned method enable the graphene transistor with unprecedented performance. The transferred method creates lots of milestone transistor performance, but there is a fatal flaw that the limitation of large scale assembly remains to be solved.

To achieve the large scale integration of top gate transistors, it is crucial to find a convenient method to overcome the challenge of ALD on pristine 2D materials. Since there is no sufficient dangling bond or nucleation site on 2D materials for the initiation of uniform dielectric deposition, the direct strategy is providing dangling-bonds and functional groups. X. Zou et al. [45] give an initial scheme by inserting an ultrathin metal oxide buffer layer as nucleation sites to improve the coverage of high-quality ALD dielectrics on MoS_2 channels (Fig. 8a). About 1 nm Y nanoparticles are evaporated on the surface of 2D materials and naturally oxidized in a drying oven. The MoS_2/Y_2O_3/HfO_2 stack presents minimized pinholes and a compact surface as shown in the inset of Fig. 8b. The fabricated device exhibits a high carrier mobility of 63.7 cm^2 V^{-1} s^{-1} and a large on/off ratio exceeding 10^8. By further scaling down the HfO_2 dielectric to 9 nm, a near-ideal sub-threshold slope (65 mV/dec) is achieved in Fig. 8b, indicating the excellent interface quality and scalability.

However, the metal oxide buffer layer introduces an extra thickness, which will reduce the capacitance of the top gate dielectric and goes against with the purpose of the application of high-k dielectric. Hence, it is important to develop a method for direct deposition of high-k dielectric without buffer layer. J. Wang et al. [43] employ a UV-O treatment to functionalize the MoS_2 surface and scale the gate dielectric down to 6 nm, fabricating the thinnest gate dielectric for MoS_2 transistors (Fig. 8c and d). The rapid 30 s treatment and the N_2 protective gas protect the 2D material from too much oxidation and mobility decline. The traps and the lattice damage induced by UV-O plays an important role in the uniform deposition of HfO_2 without extra thickness added to degrade the capacitance. By controlling the treatment time, the damage of channel materials and the degradation of channel performance can be controlled in a small range. The fabricated device confirms the high quality of the 2D/dielectric interface, showing a mobility of 46 cm^2 V^{-1} s^{-1} and a significant drain current density of 612 μA/μm.

As mentioned above, the damage of semiconductors and the reduction of performance are small, but the degradation still exits. To avoid such degradation, CVD hBN [46,115] is used as a ultrathin buffer layer (Fig. 8e and f). The hBN can be largely prepared and the defects on the surface can be controlled by the CVD process to act as dangling-bonds for the uniform ALD process. The cover process of hBN is a van der Waals approach which is widely employed in the non-damage interface. In the cross-sectional TEM image (Fig. 8f), a perfect lattice structure and an uniform interface are exhibited. In the above sections, it is mentioned that hBN is atomically thin and can effectively minimize the traps, the defects and the external scattering. So the insertion of hBN can further enhance the quality of the interface and optimize the performance of the transistor in every aspect. The obtained transistors show both obvious mobility enhancement and superior gate control. The top gate MoS_2 transistor exhibits a mobility of 88 cm^2 V^{-1} s^{-1} and an excellent sub-threshold slope (78 mV/dec). In addition, the top-gated graphene transistor with the same h-BN/HfO_2 dielectric engineering scheme also yields a mobility of 7400 cm^2 V^{-1} s^{-1} and a maximum output current density of 2.9 mA μm^{-1}. The excellent

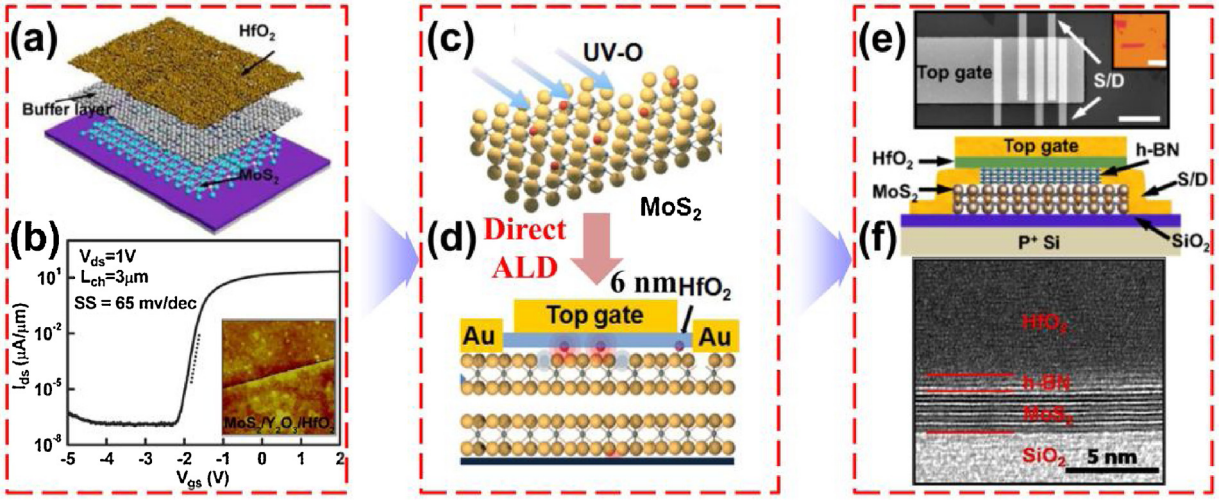

Fig. 8. (a) Structural schematic of few layer MoS_2 covered with the metal oxide buffer layer and HfO_2 film. (b) Transfer characteristics of 3 μm MoS_2 transistors. Reprinted from Ref. [45] with permission by John Wiley and Sons. (c–d) The assembly process of top gate devices with UV-O treatment. Reprinted from Ref [43]. with permission by John Wiley and Sons. (e) Illustrative schematic and SEM image of a top-gated MoS_2 FET with the hBN/HfO_2 dielectric stack. The upper inset shows the optical image of few-layer MoS_2 employed for the device fabrication. All the scale bars are 5 μm. (f) Cross-sectional HRTEM image of a SiO_2/MoS_2/hBN/HfO_2 stack with 16 nm thick ALD HfO_2 on CVD hBN. Scale bar is 5 nm. Reprinted from Ref. [46] with permission by John Wiley and Sons.

experimental data demonstrates the high quality of the fabricating device.

2.3 Surface doping engineering (2D/adsorbate interface)

For various application especially complementary device operations, it is necessary to tune the electronic properties of 2D materials through surface doping. Several doping methods have been utilized for their utility in achieving bipolar carrier conduction in 2D materials. The doping methods are classified into chemical method and physical method by dopants. The chemical method is simply controllable but instable, while the physical method is effective but induces extra traps.

2.3.1 Chemical method

Chemical method is a way to use a certain chemical reagent to spin or dip on top of the channel surface, which is simply controlled. In Fig. 9a, W. Yu et al. [116] have tested the surface chemical doping effect on the band gap opening and the vertical displacement field of the bilayer graphene FET doped by using benzyl viologen (BV) molecules. Chemical doping in bilayer graphene modulates an additional offset voltage and the band gap opening in bilayer graphene. The on/off ratio in the bilayer graphene transistors is increased and Dirac points are tuned, which can be readily configured into functional devices, such as complementary inverters. Another dopant, $AuCl_3$ [117], is used in MoS_2 FETs in Fig. 9b. The pristine MoS_2 device displays a typical n-type behavior, which is consistent with previous reports in Fig. 9c. After $AuCl_3$ doping, a high performance p-type MoS_2 FET is obtained with on/off ratio exceeding 10^7 for the Fermi level shift induced by hole carriers. The inset is the optical image of the MoS_2 device. Through introducing a graphene buffer layer, the room temperature hole mobility can reach up to 72 $cm^2\ V^{-1}\ s^{-1}$ and a low contact resistance of 2.3 kΩ· μm. The significant doping result shows a great potential in the practical application.

2.3.2 Physical method

D. Sarkar et al. [118] investigate the doping effect in 2D materials caused by nanoparticles (NPs) of different noble metals (Au, Ag, Pd, Pt) and low work function metals (Sc and Y) (Fig. 9d). It is observed that most doping exhibits p-type doping except Y. Pt NPs lead to the highest doping that the threshold voltage shift can reach up to 137 V for the highest work function. And the transfer characteristics of the MoS_2 can be gradually shifted by increasing the dose of NPs. Similarly, the Cu NPs is deposited on BP resulting in a n-type doping (Fig. 9e and f). The Cu doped BP [119] shows a positive threshold voltage shift and an increased electron mobility of 380 $cm^2\ V^{-1}\ s^{-1}$ at room temperature in Fig. 9f. The inset is the same date on a logarithmic scale. The 2D complementary inverter employs a single BP crystal with a pristine p-channel and Cu-doped n-channel, exhibiting a gain of 46. These works confirm that the 2D materials can be applied in logic circuit by further improved doping method.

2.4 Intercalation engineering (2D/2D interface)

In the above sections, we discussed the 2D/metal interface, 2D/dielectric interface, and the 2D/adsorbate interface, which are the heterojunctions between the 2D materials and other different materials. However, the layered 2D materials consist of several atomic thin films bonded by van der Waals force. The interface between interlayers is always neglected. Here, this homojunction between the interlayers is discussed.

For perfectly modulating the 2D materials performance, many novel approaches are tested. The traditional ion implantation techniques for carrier doping is a high energy process and hinders device development for the damage of 2D materials. And the surface doping engineering is currently in test phase that cannot be applied in practice. So Y. Gong et al. [120] and C. Wang et al. [121] provide an extraordinary intercalation approach which only embeds or absorbs molecules, ions and other low dimension materials into the interlayer to modulate the properties of semiconductors. These methods can retain a clean external surface of semiconductor channel toward top gate structure.

Fig. 10a demonstrates a solvent-based intercalation method to achieve p-type, n-type and degenerately doped semiconductors in the same parent material at the atomically thin limit. The pristine bilayer SnS_2 with a van der Waals gap is a natural n-type semiconductor for the S-vacancy [122–124]. After intercalating Cu into the van der Waals gap, Cu-intercalated SnS_2 acts as a p-type semiconductor and displays a hole mobility of 40 $cm^2\ V^{-1}\ s^{-1}$. With the same process, the obtained Co-intercalated SnS2 exhibits a metallic behavior and can play a role of metal. Combining this intercala-

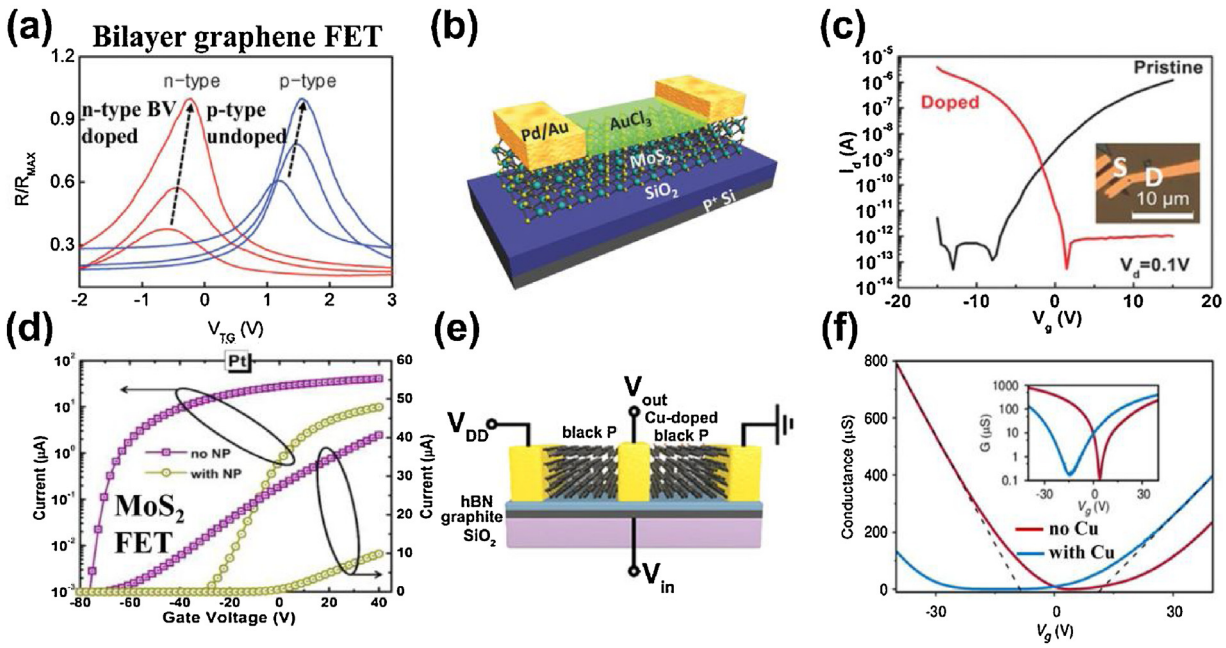

Fig. 9. (a) Switching behavior of n-type (n-type BV doped) and p-type (p-type undoped) bilayer graphene FETs. Reprinted from Ref. [116] with permission by American Chemical Society. (b) Schematic diagram of MoS_2 device and the $AuCl_3$ doping method. (c) Logarithmic scale transfer curves of a pristine MoS_2 device and its p-type transfer characteristics after $AuCl_3$ doping. The inset shows an optical microscopy image of the device. Reprinted from Ref. [117] with permission by John Wiley and Sons. (d) Drain current as a function of gate voltage for MoS_2 FETs before and after incorporation of nanoparticles of Pt. Reprinted from Ref. [118]with permission by American Chemical Society. (e) Schematic of the BP inverter fabricated using an untreated channel and a Cu doped channel. (f) Four-point conductance versus gate voltage before (red) and after (blue) Cu doping. The inset shows the same data on a logarithmic scale. Reprinted from Ref. [119] with permission by American Chemical Society.

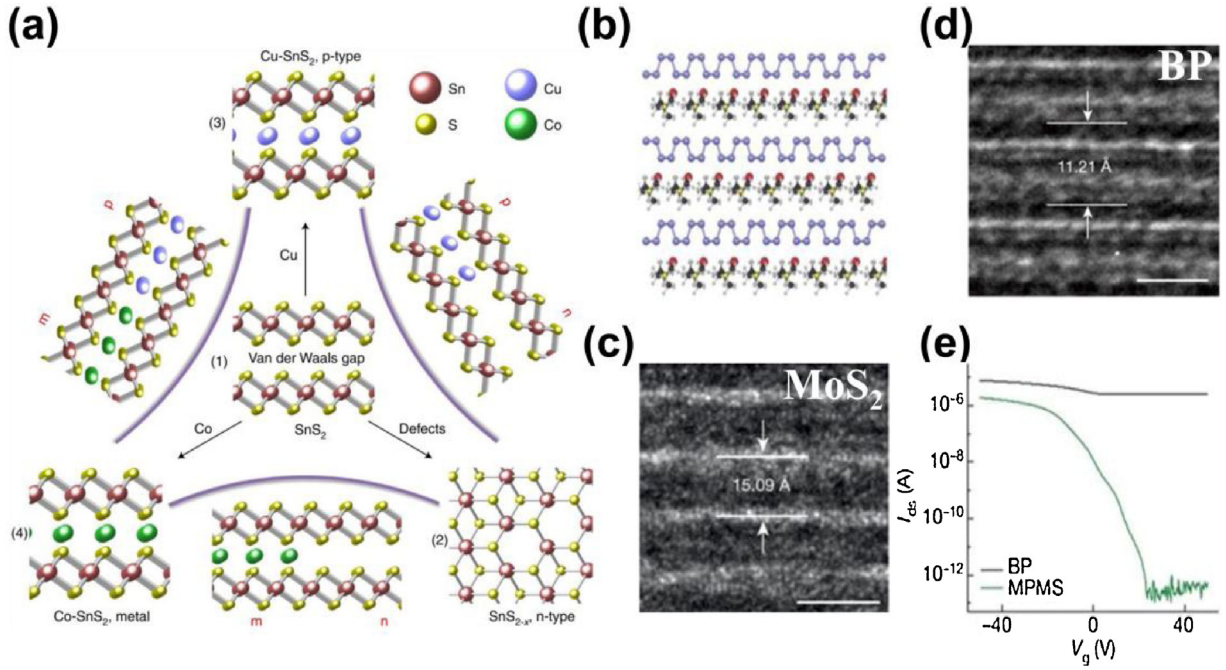

Fig. 10. (a) Schematics showing: (1) Bilayer pristine SnS_2 with a van der Waals gap. (2) The S vacancy is the dominated defect type in the naturally CVD-grown SnS_2, leading to an n-type semiconductor. (3) Cu-intercalated SnS_2 as a p-type semiconductor. (4) Co-intercalated SnS_2 as a highly conductive metal. Reprinted from Ref. [120] with permission by Springer Nature. (b) Schematic illustration of the atomic structure of MPMS. (c) The cross-sectional HRTEM image of BP/CTAB superlattice. Scale bars: 1 nm. (d) Cross-sectional TEM image of MoS_2/CTAB superlattice. Scale bars: 2 nm. (e) Transfer characteristics of MPMS show an on/off ratio >10^7 versus <10 in pristine BP device. Reprinted from Ref. [121] with permission by Springer Nature.

tion technique with lithography, an atomically seamless p–n–metal junction could be further realized with precise size and spatial control, which makes in-plane heterostructures practically applicable for integrated devices and other 2D materials. Therefore, the presented intercalation method can open a new avenue connecting the previously disparate worlds of integrated circuits and atomically thin materials.

For example, the monolayer BP is unstable and difficultly exfoliated, so the expected intrinsic properties of monolayer BP are limited. Through intercalation with cetyl-trimethylammonium

bromide (CTAB), monolayer BP molecular superlattices (MPMS) are created with an artificial superlattice structure [121] that monolayer atomic crystals alternate with molecular layers shown in Fig. 10b. The cross-sectional TEM image shows the interlayer distance (11.21 Å) is more than double of that in BP (5.23 Å), indicating the intercalation with CTAB effectively decouple the atomic layers. The new structure of BP overcomes the difficulty in isolating and stabilizing monolayer BP [125,126] to allow access to monolayer BP characteristics. For the isolation of the BP monolayers, the on/off ratio exceeds 10^7, shown in Fig. 10e. This method also can be expanded to other 2D materials, such as MoS_2. The interlayer distance is extended to 15.09 Å in Fig. 10d. These studies define a versatile material platform for fundamental studies and potential technological applications.

3 Summary

In summary, we review the recent interface engineering approaches for 2D semiconductor transistors towards high-quality fabrication technologies and high-performance electronic. Four types of interfaces in 2D material field-effect transistors are discussed in detail, including the 2D/metal contact, 2D/dielectrics, 2D/adsorbate and 2D/2D interface. For contact barrier modulation, van der Waals contacts have been demonstrated to be an effective way to eliminate pinning effect with much reduced contact resistance, which significantly improves the electronic properties of 2D FETs. To suppress the external scatterings induced by impurities and traps during the carrier transport, special issues are introduced to state the strategies for remitting the challenges in the dielectric engineering section. Moreover, the corresponding methods are introduced to overcome the non-dangling bond nature of 2D materials, which make difficulties for dielectric deposition. With the advanced integration technologies, the CVD hBN buffer layer scheme provides a nearly perfect strategy which not only acts as a nucleation site for ALD but also forms a compact and uniform interface, meanwhile, the hBN encapsulation screens the external scatterings, thus the device performance is further optimized. For creating more functions, the modulation of 2D materials' properties is necessary. Surface doping at the 2D/adsorbate interface has been demonstrated as an effective method to tune the device performance. To further achieve a better doping method without disturbing other interface engineering, the intercalation approach is introduced that the doping adsorbate is in the van der Waals gap of interlayers, showing a novel effect on electronic properties. The performance of 2D FETs is continuously improved by bettering the device interfaces.

Although great advance has been made in this yield, the practical application of 2D FETs still has many challenges. Due to large surface/volume ratio of atomically thin 2D materials, 2D FETs are susceptible to interfaces disorders, thus interface engineering is a critical issue in 2D devices. Although numerous physical assembly van der Waals integration approaches are reported to fabricate 2D FETs without lattice damage to protect the intrinsic electrical properties of 2D materials, the best performance of 2D FETs is far from ideal and barely comparable to that of state-of-the-art silicon devices. This result indicates that there is still plenty of room for improvement in device fabrication technologies without interface damage to realize 2D FETs with optimal performance. Moreover, present optimizing works are primarily based on single transistor with the mechanically exfoliation 2D material nanosheets, further studies are called for repeating them on large-area synthesized 2D materials to realize large-area integration and the synthesis of 2D materials has to be developed to overtake the performance of mechanically exfoliation 2D materials. To this end, to make 2D transistor be possible for functional electronics, it is emerging to integrate it with other material systems based on current materials and fabrication technologies. In addition, the discovery of new materials and the design of new concept transistors are also equally required for future application and manufacture. Except unique electrical properties, 2D materials are good system for optoelectronic response for their tunable bandgap. With the deepening of theoretical research and experiments, more technology difficulties will be overcame and 2D FETs will show a broader application prospect.

Acknowledgments

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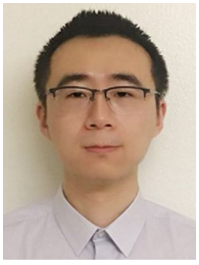

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